SINGLE DC SOURCE-BASED MULTILEVEL CONVERTER TOPOLOGY WITH REDUCED POWER SWITCHES AND CONDUCTION LOSSES

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Abstract: *Nowadays multilevel inverter with reduced switch count is more attractive among the researchers due to the unsuitability of the conventional multilevel inverter where the installation space is constrained. In this category, the marine ship board has limited installation space. In this paper, a new multilevel inverter with reduced power electronics components with improved conduction loss is proposed. The proposed topology is compared with conventional and recent multilevel inverter topologies in terms of the number of levels, auxiliary diode, gate driver circuits, and blocking voltage of switches. The performance of proposed multilevel inverter is measured by using simulation software MATLAB/Simulink, and laboratory workbench-based experimental test has been conducted. Finally, the comparison between the simulation output and experimental result is discussed to prove the superiority of proposed topology.*

Key Words: *Multilevel Inverter, Total Harmonic Distortion, Shipboard, Symmetric topology*

Introduction

Renewable energy source applications are widely used in all the industries including marine, automobile, traction, and the utility grid. Various renewable energy source applications are available such as photovoltaic (PV) system, wind energy, hydro energy, fuel cell (FC), and biomass. The overview of marine electrical system network is shown in Figure.1. The power converters are playing a major role to control the drive system, communication system, and lighting applications. The electrical system with a combination of ship services and propulsion has significantly reduced the cost and increased the flexibility [1]. Instead of single blocks for each electrical control unit, the power electronics building block (PEBB) contains all together in a single unit, which leads to reduction in the weight, size, and cost of the system [2].

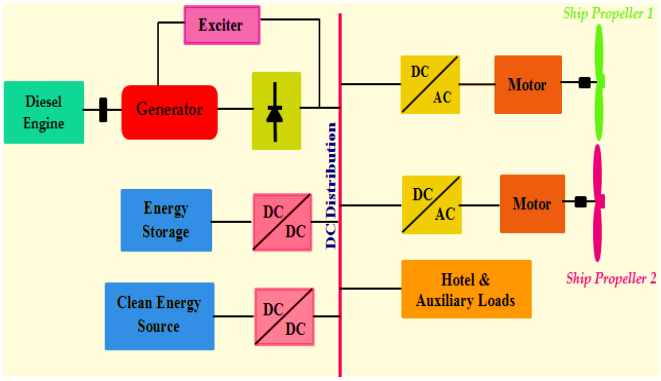


Figure.1 Schematic Diagram of Ship Propulsion Electrical System

Both DC and AC power converters are used with PWM techniques, which minimizes the harmonics and filter size, but the switching losses are high [3]. Power quality is a major issue among others such as abnormal voltage, frequency variations, harmonics, and transients in a shipboard power plant, which is addressed in [4]. The battery-based shipboard is environmental free, but the size of battery bank will increase the cost of the system. The hybrid energy sources like diesel, photovoltaic, and fuel cell are in conjunction with battery to operate the small- to medium-sized shipboards [5]. Photovoltaic-powered shipboard and issues related to the electrical network are addressed in [6]. A hybrid power system based on PV/FC/diesel generator system is proposed and modeled for green energy and compared with conventional shipboard electrical power generation [7]. The multilevel converters have advantages such as low dv/dt stress, low total

harmonic distortion, low electromagnetic interference (EMI), and several multilevel converters for shipboard, and the technical challenges of high-power marine system related to power converter topology are source side power quality and switching device limitations [8]. The conventional multilevel inverter topologies are (i) cascaded H-bridge (CHB), (ii) neutral point clamp (NPC), and (iii) flying capacitor (FC). The drawback of the two-level inverter in shipboards is the design of LC filters for line side, high-power semiconductor devices, high switching frequency, and high common voltage problem [9]. In[10], the suitability of conventional multilevel converter in various applications in shipboard is discussed.

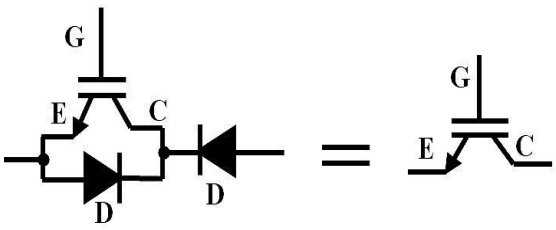
The flying capacitor multilevel converter drive induction motor in shipboard is presented in [11], and this offers better dynamic performance and easy modulation scheme [12]. Even though the conventional multilevel converters have numerous advantages, the unique disadvantage of conventional topologies is used in a higher number of switches. Several new multilevel inverter topologies with reduced switches are presented in [13-16]. A diode-based novel multilevel converter topology with reduced power electronics components are addressed in [13], and the switches with the series connection of diode are presented. The single dc source with multiple dc-link capacitors and bidirectional switches are used to minimize the number of switches in [14]. The unidirectional switch with the parallel connected diode is presented in [15], and also to reduce the high blocking voltage, full bridge inverter is hybrid with proposed topology. Several basic units are connected in cascade for both symmetric and asymmetric configurations as presented in [16] to produce stepped output voltage at the load. In [17], it is proposed for seven levels with reduced switches, but this topology is limited to seven levels if the number of level increases the required number of switch, and power diode also increases with increasing switching pattern complexity. New asymmetrical multilevel converter topology is presented in [18], and also, cascaded topology of proposed converter is discussed. Other than these topologies, several multilevel converters are presented in [19-20]. However, these topologies have unique pros and cons as follows:

(i) Single DC source (non-isolated DC source) with multiple dc-link capacitors
(ii) Bidirectional switches
(iii) Low On-state switches
(iv) Suitable for PV and wind applications
(v) Not equal power sharing
(iv)Various voltage rating switches

However, these topologies require more power semiconductor devices like IGBTs or MOSFET and power diode. In order to minimize the power semiconductor components, in this paper is proposed a novel multilevel converter topology. The following sections are constructed as (i) proposed topology, (ii) mathematical modeling of proposed topology is presented, (iii) various losses associated with proposed multilevel inverter are discussed, (iv) proposed topology with comparison of recent topologies is graphed to show the required number of switches and blocking voltage, (v) to prove the authority of proposed topology, a simulation and experimental-based results are presented, and (vi) finally, the superiority of proposed topology and suitable applications are stated.

Proposed Topology

In this section, the construction of proposed symmetric topology with a number of power electronics components is discussed. Figure 1 illustrates the IGBT with the series connection of a diode and without anti-parallel diode switch. Without anti-parallel diode, the switch does not provide a freewheeling path to the current, which introduces a spike at the load, but some topologies are designed as a switch with the series connection of diode that also does not provide freewheeling path except neutral point clamp because of neutral mid-point. Most of the topologies require IGBT with anti-parallel diode, but the topologies shown in Figure 2 use IGBT with anti-parallel diode and series connection of diode. The switched diode multilevel inverter topology also does not provide freewheeling path because unidirectional switches are connected in series with IGBTs.

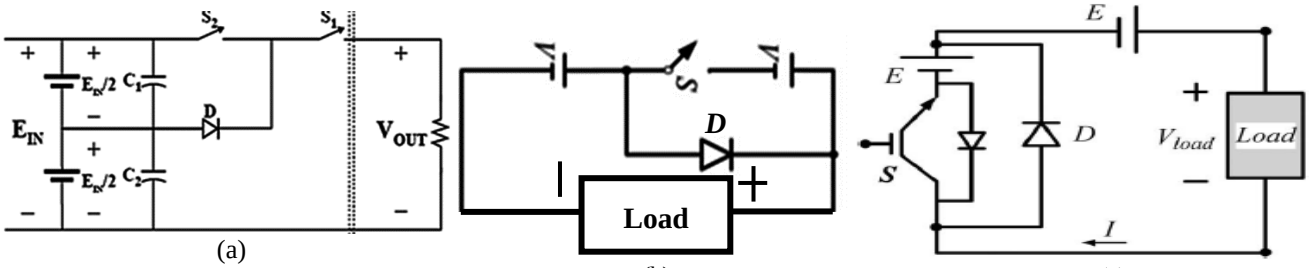


(a) (b)

Figure.2 (a) Switch with anti-parallel diode and series connected diode and (b) switch without anti-parallel diode used in proposed topology

In Figure 3, different basic unit of the multilevel inverter is used in [13],[[15-16]. The proposed topology is recommended to use without anti-parallel diode because the conduction losses across the diodes will be reduced double time than [13-16]. In [13], the diodes are placed between the two capacitors and connected with switches. When the switches are turned, the corresponding capacitor voltage will occur at the load and current flow through the diode and switch to the load. The topologies consist of "N" number of dc sources with parallel connected diode except for the first dc source in [15].

divided into two parts (i) level producer part and (ii) alternator part. The level producer part consists of single dc source (V_{in}) with several dc-link capacitors (C_1, C_2….C_n) connected to switches without freewheeling diode (S_1, S_2…….S_n) in between, and these switches are directly connected with an auxiliary switch (AS) as shown in Figure.4. The auxiliary switch (AS) consists of the anti-parallel diode to provide the continuous current path in zero states. The generalized switching sequence for "m`" number of levels is listed in Table.1, and the sequence is presented for "2N+1" levels.



(a) (b) (c)

Figure.3 (a) Basic Unit Proposed in [13], (b) Basic Unit proposed in [15] and (c) Presented basic unit in [16]

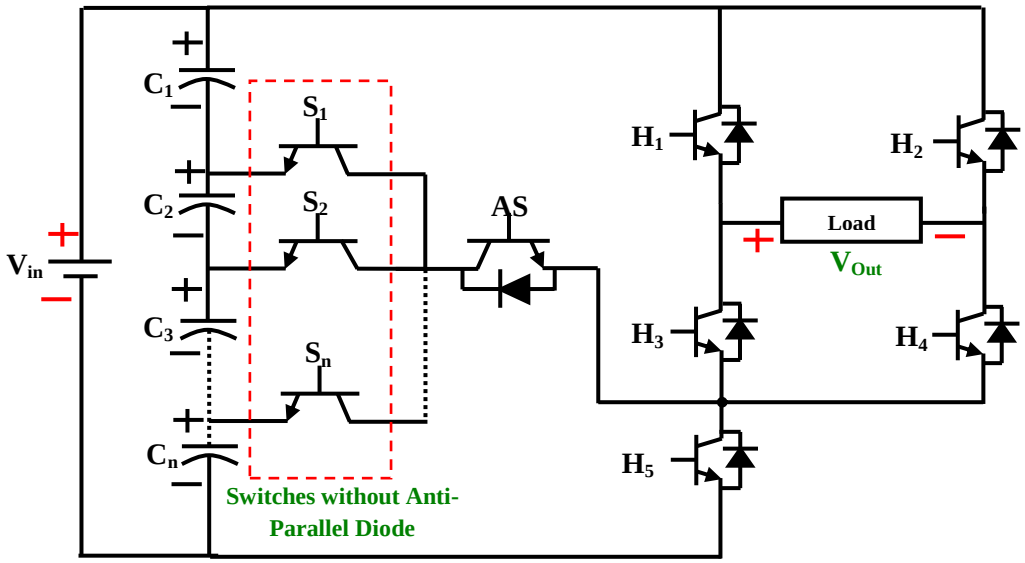


Figure.4 Generalized Structure of Proposed MDCC Multilevel Inverter

These topologies are configured for both symmetric and asymmetric configurations. The proposed topology is only suitable for symmetric configuration, so the symmetric configuration of other topologies is only considered in this paper. Here it is worth to mention that proposed topology requires less number of power electronics components than other topologies. The proposed converter uses a lower number of switches to obtain a higher number of levels, and this topology is

This proposed multilevel inverter is called as multiple DC-link capacitor-based multilevel inverter (MDCC MLI) topology. The V_{in} value is equally divided into each capacitor such as V_{in}/N, where N is the number of capacitors. Each dc-link source magnitude is equal since this topology is only suitable for symmetric configuration. The nature of a capacitor will not maintain the equal voltage among the each capacitor, so the voltage balancing circuit is required [21] for proposed topology.

Alternator part requires four switches (H_1-H_4) that are capable of high blocking voltage to produce synthesized stepped positive and negative output voltages (0, $\pm C_1$, $\pm C_2$……$\pm C_n$) at the load.

Table 1. Switching Sequence for Proposed Topology

Level	Switches OFF	Switches ON	Output Voltage	Number of On-State
0	H_3,H_4,H_5 or H_1,H_2	H_1,H_2 or H_3,H_4,H_5	0	2 or 3
1	H_2,H_3,H_5 S_2…S_n	H_1,H_4, AS,S_1	$+C_1$	4
2	H_1,H_4,H_5 S_2…S_n	H_2,H_3,AS,S_1	$-C_1$	4
3	H_2,H3,H_5 S_1,S_3…S_n	H_1,H_4, AS,S_2	$+C_1+C_2$	4
4	H_1,H_4,H_5,S_1,S_3…S_n	H_2,H_3,AS,S_2	$-(C_1+C_2)$	4
5	H_2,H3,H_5 S_1,S_2,S_4…S_n	H_1,H_4, AS,S_3	$+C_1+C_2+C_3)$	4
6	H_1,H_4,H_5,S_1,S_2,S_4…S_n	H_2,H_3,AS,S_3	$-(C_1+C_2+C_3)$	4
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮
2N	H_2,H3,H_5 S_1,S_3…S_n	H_1,H_4,S_5	$+\sum_{i=1}^{n} C_n$	3
2N+1	H_1,H_4,H_5,S_1,S_2,S_4…Sn	H_2,H_3,S_5	$-\sum_{i=1}^{n} C_n$	3

The C_n capacitor is connected to the load through switch H_5 remaining in all the capacitors that are connected through AS and switches (S_1-S_n). The number of output voltage levels(N_{Level}), number of IGBTs with anti-parallel diode ($N_{IGBT,D}$), number of IGBTs without anti-parallel diode(N_{IGBT}), number of gate drive circuits(N_{Gate}), and total blocking voltage of proposed inverter are discussed as follows:

The number of levels based on the dc-link capacitor is expressed in equation (1)

$$N_{Level}= 2N+1 \quad (1)$$

Number of IGBTs with and without diode can be calculated by using equations (2) & (3)

$$N_{IGBT}= N-1 \quad (2)$$

$$N_{IGBT,D}= 6 \quad (3)$$

The total number of IGBTs is considered as switches and can be evaluated as follows:

$$N_{Switch}=N+5 \quad (4)$$

The required number of gate driver circuits and total blocking voltage are expressed in equations (5) & (6)

$$N_{Gate}= N+5 \quad (5)$$

$$T_{Block}= V_{dc} * (P+2N) \quad (6)$$

where $P= 3N^2/4$ for even number of N

$= (3N^2+1)/4$ for odd number of N

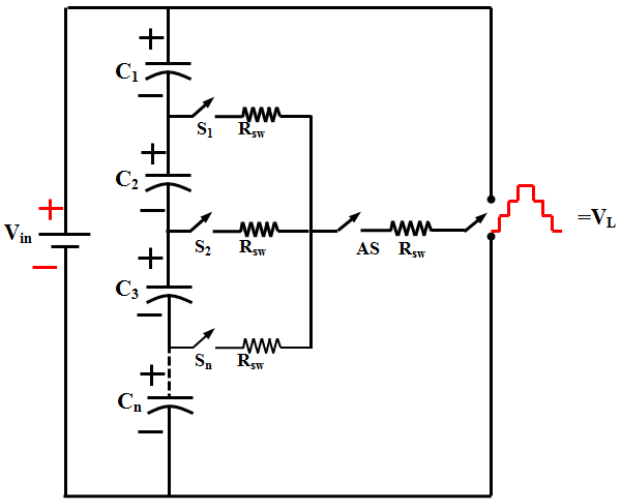
where "N" is the number of dc-link capacitors. The comparison of proposed and conventional H-bridge multilevel inverters for symmetric configuration is listed in Table.2. Comparison of the number of switches, state switches, blocking voltage, and gate driver circuits is presented. It is evident that proposed topology uses a lower number of switches for a higher number of level.

Table.2 Comparison of proposed and cascaded H-bridge multilevel inverters for symmetric configuration

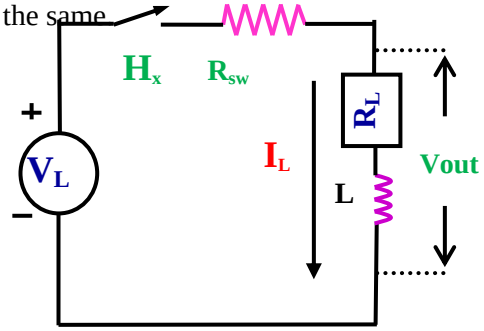
Description	Proposed	CHB
Number of IGBTs without anti-parallel diode	N-1	-
Number of IGBTs with anti-parallel diode	6	4*N
On-state switches	4	2*N
Total blocking voltage	V_{dc} * (P+2N) Where $P= 3N^2/4$ for even number of N $= (3N^2+1)/4$ for odd number of N	$4*N*V_{dc}$
Number of DC source	1	N
Number of DC-link capacitors	N	-
Maximum output voltage	$N*V_{dc}$	$N*V_{dc}$
Gate driver circuits	N+5	4*N

Modeling of Proposed Multilevel Inverter

A state space mathematical model representation of any system comprises a set of input, output, and state variables state space model is a more flexible and convenient method to model and



(a)



(b)

Figure.5 (a) Topology of MDCC (b) simplified circuit for state space model

analyze systems with "n" number of inputs and outputs. Consider S_1, S_2, S_3,…AS, and H_5 be the signals for each level of output to the 9-level inverter. A simplified model and equivalent circuit of the proposed multilevel inverter is represented in Figure.5. The Figure.5a, $S_1 \ldots S_n$ are switched with internal resistance (R_{SW}), the V_L level generator output voltage, which is positive output cycle. In Figure. 5b, the Hx and Rsw are the full-bridge switch sand resistance and L and R_L are load inductance and resistance.

Let

$$B = \begin{cases} 1 & \text{for positive half cycle} \\ -1 & \text{for negative half cycle} \end{cases} \quad (7)$$

The variable "F" is the realization of the full bridge in the proposed topology; the Sx and R_{SW} are switch and switch resistance, respectively. Therefore, the net output V_L from the m-level inverter is given by:

$$V_L = \begin{bmatrix} 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} B_1F \\ B_2F \\ B_3F \\ B_4F \end{bmatrix} \begin{bmatrix} V_{dc} \end{bmatrix} \quad (8)$$

where V_{dc} is the magnitude sum of each dc source and B_1 to $B_4$is the comparator output signal (binary output). By applying KVL to the circuit:

$$V_L = R_{sw} i_L(t) + R_L i_L(t) + L\frac{di_L(t)}{dt} \quad (9)$$

where R_L = R + R_{ind} and R, R_{ind}, R_{SW}, and L are the total load resistance in ohms, the load resistance in ohms, the internal resistance of a load inductor in ohms, the ON-state resistance of the total conducting IGBTs in each level, and the load inductance in mH, respectively. In this topology, in each level, the number of conducting components is the same.

$$L\frac{di_L(t)}{dt} = \begin{bmatrix} 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} B_1F \\ B_2F \\ B_3F \\ B_4F \end{bmatrix} \begin{bmatrix} V_{dc} \end{bmatrix} - (R_{sw} + R_L) i_L(t)$$

(10)

Let the state variable be the current through the inductor $x=i_L(t)$ and input variable $u=V_L$:

$$\frac{di_L(t)}{dt} = \frac{\begin{bmatrix} 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} B_1F \\ B_2F \\ B_3F \\ B_4F \end{bmatrix} \begin{bmatrix} V_{dc} \end{bmatrix} - (R_{sw} + R_L) i_L(t)}{L}$$

(11)

where $\dot{x} = \frac{di_L(t)}{dt}$;

$$A = \begin{bmatrix} 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} B_1F & B_2F & B_3F & B_4F \end{bmatrix}^T$$

$$B = -(R_{sw} + R_L)$$

Similarly, the voltage across the load is given by the expression:

$$V_{out} = R_L i_L(t) + L\frac{di_L(t)}{dt} \quad (12)$$

where $y = V_{out}$; $C = (R_L + L\frac{d}{dt})$; and $D = 0$

In general, the state space switched model of the proposed topology is given by:

$$\frac{di_L(t)}{dt} = \frac{[A]\,[B_1F \quad \cdots \quad B_kF]^T\,[V_{dc}] - (R_{sw} + R_L)i_L(t)}{L} \tag{13}$$

Where the dimension of [A]=1 × (N_{level} -1)/2, *k* varies from 1 to (N_{level} -1)/2, Vdc is the magnitude of each dc source, and $i_L(t)$ is the current through the inductor. The generalized state space switched model is explained in equation (13), and it is applicable for proposed asymmetric topology with any number of levels. The various operating mode of proposed topology for nine-level inverter is illustrated in Figure.6. In this, the switches S_1……S_n will be turned ON and OFF one time for each half cycle with auxiliary switch and full bridge switches either (H_1& H_3) or (H_2& H_4) pair. The positive cycle and negative cycle of current flow are indicated in red and blue colors, respectively.

Loss In Proposed MDCC MLI

The switching and conduction losses [13] are a major loss in the multilevel converter, and also the proposed topology consists of multiple dc-link capacitors, so the loss of capacitors is also taken into account.

A. Loss in Switch Conduction Mode

(i) Conduction Loss

The duration of ON period of switches is taken into account, and the voltage drop across the switch during on period is based on the semiconductor used in the switch, and this is available from manufacturer datasheet. Conduction losses are calculated for both IGBTs ($P_{C,T}$) and anti-parallel diode ($P_{C,D}$) as in equation (14). It is evident that proposed topology produces low conduction loss because it does not require anti-parallel diode-based switches except six switches. The resistance on the semiconductor and voltage drop is multiplied with current through the switches as given in expressions (15) and (16).

$$P_C = P_{C,T} + P_{C,D} \tag{14}$$

$$P_{C,T=}[V_{on,T}(t) + R_T.I^{\beta}(t)].I(t) \tag{15}$$

$$P_{C,D=}[V_{on,D}(t) + R_D.I(t)].I(t) \tag{16}$$

β- is the constant specification-related transistor, and it is available from manufacturer datasheet, $V_{on,T}$ and $V_{on,D}$ are the constant parameters, on state voltage of transistor and diode, respectively. The advantage of proposed topology is low conduction losses because the switches S1...Sn do not have the anti-parallel diode. The comparison of conduction loss and other topologies is illustrated in the graph as shown in Figure.7.

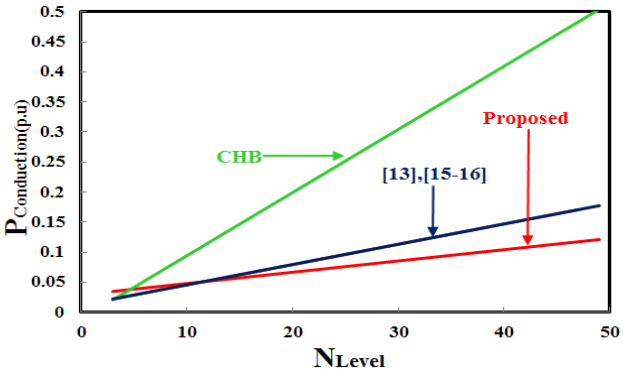


Figure.7 Conduction Loss Vs Number of Level

(ii). Switching Loss

The expression for energy loss during the turn on (E_{ON}) and turn off (E_{OFF}) of switches is:

$$E_{OFF} = \frac{V_{off}.I.t_{off}}{6} \tag{17}$$

$$E_{ON} = \frac{V_{off}.I.t_{on}}{6} \tag{18}$$

where t_{on} and t_{off} are on and off state time of switches, V_{off} is voltage across the switches in off state.

$$P_{SW} = 2f(E_{ON} + E_{OFF}) \tag{19}$$

The above equations (17) and (18) give energy losses for one switch, and the resultant equation (19) gives switching loss of single switch, in order to calculate the switching losses for all the switches presented in multilevel inverter of the equation (20) used.

$$P_{SW} = 2f(\sum_{i=1}^{n} E_{ON,i} + E_{OFF,i}), \tag{20}$$

Where n- is the last switch of the proposed multilevel inverter.

However, both conduction and switching losses depend on the voltage and current ratings of switches, but in recent topologies, the voltage rating of switches is variable and current is equal in all the switches. The voltage ratings of switches are chosen based on the blocking voltage across the switches. In this paper, the switching losses are not provided because the proposed topology requires a minimum number of switches and operates under fundamental switching modulation techniques. The proposed topology uses a low number of switches compared

to topologies [13-16]. Figure.8 depicts the switching loss of proposed topology against a number of levels. The energy loss during turn on and turn off is directly proportional to the blocking voltage from this, if the blocking voltage increases, the switching loss also increases. Conventional CHB has low blocking voltage compared to proposed topology and [13-14].

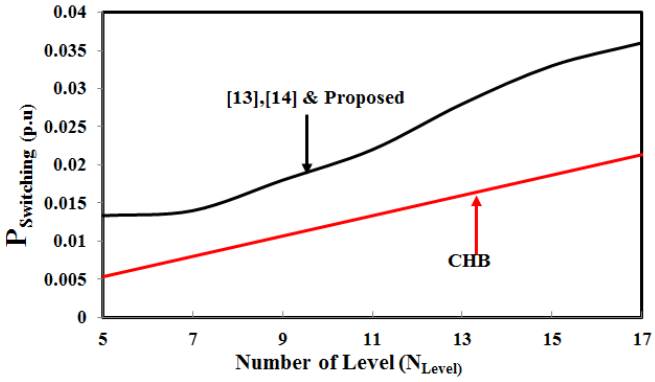


Figure.8 Switching Loss Vs Number of Level

B. Capacitor loss

In power electronics, circuit's most common failure components is a dc-link capacitor, which has losses based on heat dissipation and reduces the reliability of the system. The major capacitor losses are due to voltage stress, excessive operating voltage, reverse voltage, and excessive ripple current. These factors are an influence to increase dissipation factors of the capacitors as presented in [22], and capacitor design is considered based on reliability, and life time capacitor is based on their applications [23]. In this paper, the capacitor losses are not considered because all the topologies require same number of DC-link capacitors in input side.

$$\tan\delta = \frac{R}{1/\omega C} = \omega CR \qquad (21)$$

$\omega = 2\pi f, \pi -$ Circular Constant, f - Frequency

R- Equivalent series resistance of capacitor

The total power losses in proposed topology is

$$P_{LOSS}=P_C+P_{SW}+P_{CAP} \qquad (22)$$

Figure.9 illustrates the comparison of total power loss excluding the capacitor loss because the capacitor loss in all the topology is same.

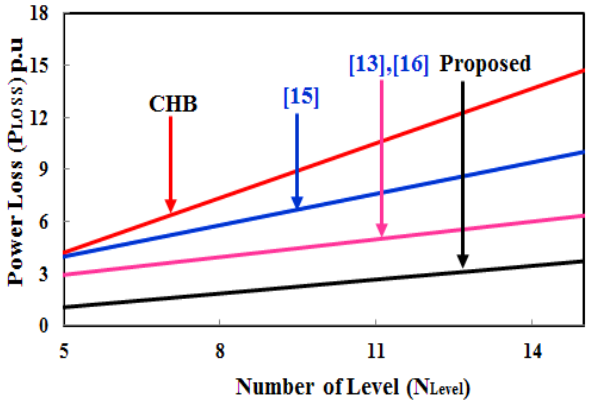


Fig.9 Number of Level (N_{Level}) Vs Power Loss (P_{LOSS})

Figure.9 illustrates the comparison of total power loss excluding the capacitor loss because the capacitor loss in all the topology is same. In general, the switching loss value is lower than the conduction loss. In this, CHB has high conduction loss due to large number of on time switches and diode. The proposed topology may produce high switching loss, but the conduction loss is low, which further reduces the total power loss.

Comparison with Other Topologies

(a) Required Number of Switches

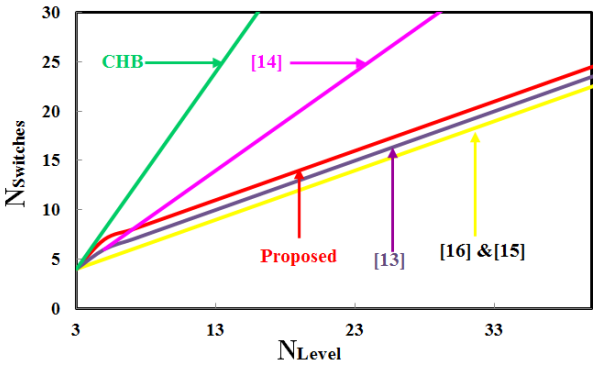


Figure.10 Number of Switches Vs Number of Level

The superiority of proposed topology can be proved by comparing the topologies [13-16] and CHB; the number of switches and number of level is shown in Figure.10. The topologies [13],[15] and [16] use a low number of switches because the dc source is connected with series of IGBT and parallel/series to the diode. The conventional CHB presented in [14] requires a higher number of switches than the proposed.

(b) Required Number of Power Semiconductor Devices

Table 3 Comparison of number of power components required for 9-level inverter

S.No	Description	Proposed	[13]	[14]	[15]	[16]	CHB
1.	Number of switches	9	8	10	7	7	16
2.	Anti-parallel diode	6	8	10	7	7	16
3.	Number of Diode	-	3	-	3	3	-
	Total Number of Components	15	19	20	17	17	32

Another important parameter related to reliability is a total number of devices used in the circuit. Figure .11 illustrates the total number of devices against a number of levels. This proposed topology requires a minimum number of devices (IGBT and power diode) compared to all other devices. As the number of devices increases, the reliability of the inverter will be degraded. Table.3 presents the detailed components required for a 9-level inverter with each topology.

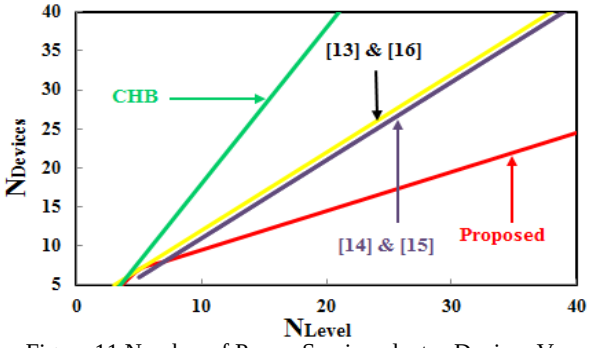


Figure.11 Number of Power Semiconductor Devices Vs Number of Level

The topologies [15-16] and proposed topology require a minimum number of power electronics components such as number dc-link capacitor, power diode, and switches. In general, the conduction loss value is higher than the switching loss; here it is worth to mention that proposed topology requires a minimum conduction loss compared to [15-16]. To reduce the switching loss, various modulation techniques are proposed [24], but for conduction loss, the semiconductor device has to change or reduce the components, hereby reducing the components by achieving the low conduction losses.

(c)Total Blocking Voltage

The withstanding voltage across the switches will be varying to each structure of multilevel inverter topology.

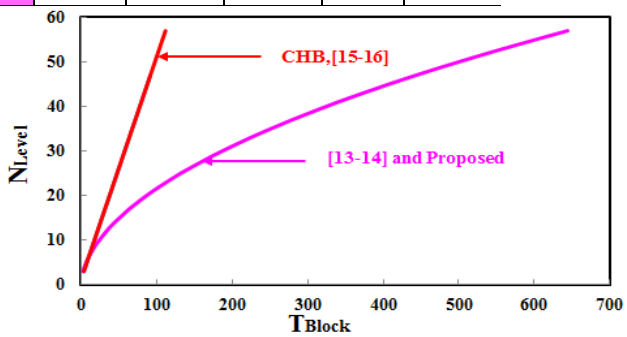


Figure.12 Number of Level vs Total Blocking Voltage

The total blocking voltage is the sum of voltage across all the switches that are taken into account; the topologies presented in [15-16] use an isolated dc source in which switch's blocking voltage is equal to each dc sources connected with them, but in the case proposed, [13-14] structures are developed based on single dc sources as shown in Figure.12. This will increase the blocking voltage across the switches. However, the proposed topology uses a lower number of power semiconductor devices and low conduction losses.

Simulation and Experimental Results

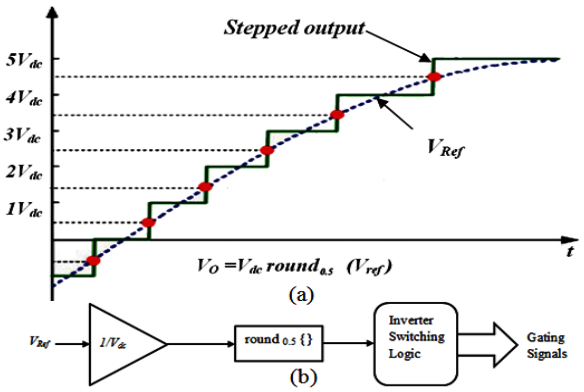


Figure.13 Nearest level selection: (a) Level synthesis and

To verify the performance of proposed topology, the simulation and experimental results are presented for a 9-level inverter. The fundamental switching

(50Hz) method called nearest level modulation (NLM) technique as illustrated in Figure.13 is used in both simulation and hardware. NLM technique has low switching frequency which produces low switching loss compared to carrier-based modulation techniques. The output voltage frequency is 50Hz, and all DC/AC power converters paid more attention to the total harmonics distortion (THD). The THD equation for the sinusoidal waveform is expressed in equation (23).

$$THD = \sqrt{\frac{\sum_{h=3,5,7....}^{\infty} V_{oh}}{V_{o1}}} = \sqrt{\left(\frac{V_{orms}}{V_{o1}}\right)^2 - 1} \qquad (23)$$

In equation (23), h (odd order of the harmonic) =3, 5, 7…. and V_{o1} fundamental of the output voltage. V_{oh} order harmonic. $V_{o,rms}$-is the rms value of the output voltage. The magnitude of the V_{o1} and $V_{o,rms}$ can be calculated using the following relations:

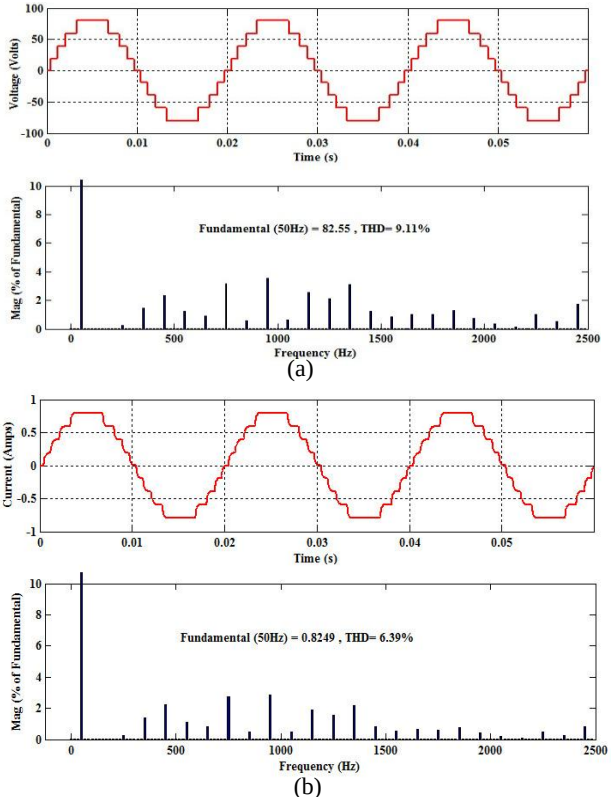


Figure.14 Simulation output results for (a) output voltage waveform and (b) current waveform

$$V_{orms} = \frac{2\sqrt{2}V}{\pi} \times \sqrt{\sum_{h=odd}^{\infty} \left(\sum_{j=1}^{N_{Level}} \frac{\cos(h\theta_j)}{h} \right)^2} \qquad (24)$$

$$V_{o1} = \frac{2\sqrt{2}V}{\pi} \times \left(\sum_{j=1}^{N_{Level}} \frac{\cos(h\theta_j)}{h} \right) \qquad (25)$$

where the values of θ1, θ2…θ_{NLevel} are switching angles and are calculated by the following equation:

$$\theta_j = \sin^{-1}\left(\frac{j-0.5}{N_{Level}}\right) \quad j=1,2,3....N_{Level} \qquad (26)$$

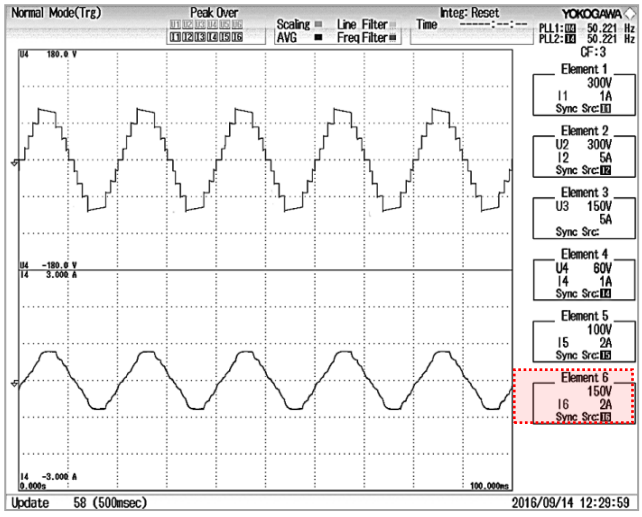


Figure.15 Experimental output Voltage and Current Waveform

Equations (24), (25), and (26) confirm that output voltage THD depends on a number of output levels and switching angle. The simulated proposed 9-level inverter output voltage and current waveform are shown in figures.14 a and b, respectively. The voltage across each dc-link capacitor is 20V. The simulation output voltage THD is 9.11% and current THD is 6.39% for R=100Ω and L=12mH, respectively. The current THD depends on the load value if highly inductive, the inductive will act as a low-pass filter and produce a sinusoidal waveform. The experimental output voltage and current waveform are shown in Figure.15. In this, IGBT BUP400D switches, maximum V_{ce} of 600V, and maximum current Ic of 22A are used. The required number of switches for the 9-level inverter is 9 switches with 9 gate driver circuits. In simulation and experimental, the input voltage and load R-L values are kept as same. It is observed that both simulation and experimental have a good agreement in terms of THD and output values. By keeping the modulation index as 80%, the output voltage level across the load is reduced to 7 levels, and 50% of modulation index produces a 5-level output voltage at the load as shown in Figure.16. The experimental results of voltage and current RMS value, total harmonics distortion for both voltage and current are presented in Figure16. The THD value of both voltage and current are 10.034 % and 7.083 %, respectively, which is in good agreement with simulation value. The theoretical value of RMS voltage for peak value of 80V is 56.56 V, in

simulation results 58.67, but in experimental 58.2V, which is once again confirming that proposed topology has good agreement with simulation and produces better results.

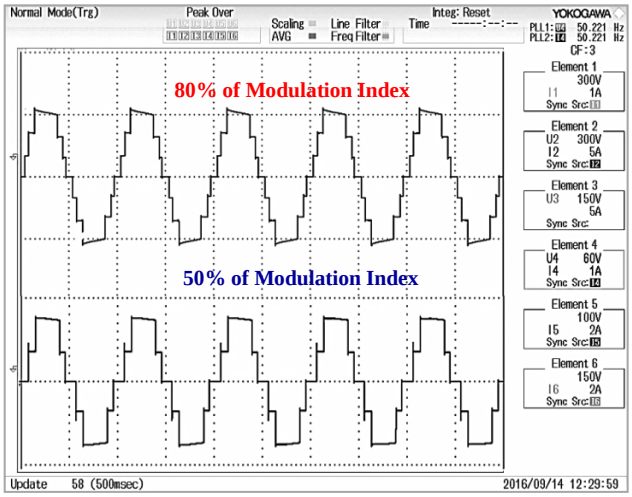


Figure.16 Experimental output Voltage Waveform for 80% and 50% modulation index

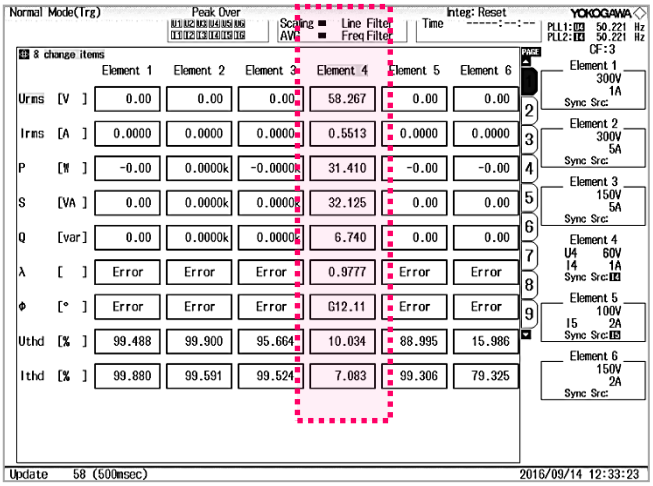


Figure 17. Experimental Power quality analyzer results of proposed 9-level inverter

The FPGA controller is used to generate the switching pulses, the output of controller is fed to the isolation circuit (optocoupler) and driver circuit to enhance the driving. The photograph of the experimental setup is shown in Figure.18 with the digital storage oscilloscope is presented and the experimental voltage and current waveforms are presented. In this FPGA Spartan, theXE3S250E controller is used to generate the switching pulses for the 9-level inverter. The efficiency of proposed topology is listed in Table.4.

Table. 4 Various Parameters measured in proposed 11-level inverter for R=100Ohm and L=12mH

Results	Vrms (V)	Irms (A)	V THD (%)	I THD (%)	Pin (W)	Pout (W)	Efficiency η (%)
Simulation	58.60	0.59	9.11	6.39	34.57	34.00	98.34
Experimental	58.26	0.55	10.03	7.083	32.04	31.41	98.03

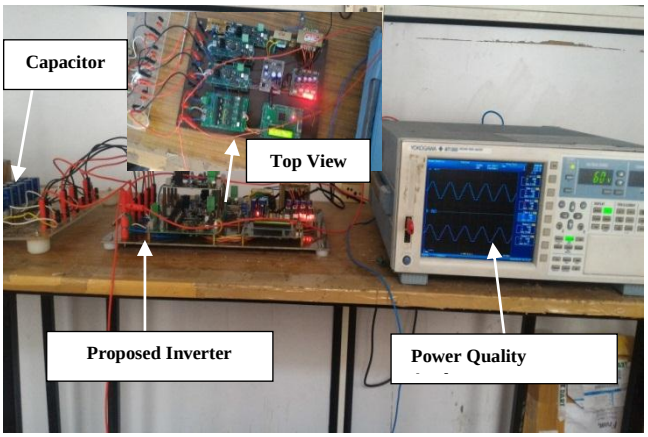


Figure.18 Photograph of Experimental Workbench

Conclusion and Future Scope of Work

In this study, a new single dc source with multiple dc-link capacitors based on symmetric multilevel inverter structure is developed. The anti-parallel diode and without diode-based switches are used, which minimizes the conduction losses. The proposed topology produces low power loss compared to other topologies for the same number of output voltage levels and it requires lower number of the power semiconductor devices, which leads to reduction in layout size, simple switching pattern, and high efficiency. Total blocking voltage of proposed topology is equal to [13-14], but higher than the CHB. Hence, the performance and efficiency of the proposed 9-level inverter are verified by both simulation and experimental results. It is evident that the proposed topology is more suitable for shipboard applications because single dc source can be used to drive the shipboard propulsion motor. The full-bridge inverter switches should withstand the maximum voltage, which increases the cost, and in order to reduce the maximum blocking voltage, cascaded structure is recommended, and this is considered as a future scope of work.

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