A SLIDING MODE CONTROL FOR POSITIVE OUTPUT ELEMENTARY LUO CONVERTER

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Abstract: *This paper studies a design of Sliding Mode Control (SMC) for Positive Output Elementary Luo Converter (POELC) operated in Continuous Conduction Mode (CCM). The POELC performs the voltage conversion from positive DC source voltage to positive DC load voltage. Due to the time varying and switching nature of POELC, its dynamic behavior becomes highly non-linear. In order to improve dynamic performances of POELC for both static and dynamic specifications, SMC is proposed. The SMC is designed by using state-space average modeling of POELC. The simulation of POELC with its control model is implemented in MatLab/Simulink. The performances of proposed controller with system are tested at various regions. The simulation results validate the effect of SMC on the static and dynamic performances of POELC.*

Key words: *DC-DC converter, positive output elementary luo converter, state-space average method, sliding mode control.*

1. Introduction

DC-DC conversion technology has been developing very rapidly, and DC-DC converters have been widely used in industrial applications such as dc motor drives, computer systems and communication equipments.

Switch-mode power converters represent a particular class of Variable Structure Systems (VSS), and they can take advantage of nonlinear control techniques developed for this class of system [1]. An ideal control should ensure system stability in any operating condition and good static and dynamic performances in terms of rejection of input voltage disturbances and load changes [2].

These characteristics, of course, should be maintained in spite of large input voltage, output current, and even parameter variations (robustness) [3].

A classical control approach relies on the state-space averaging method, which derives an equivalent model by circuit-averaging all the system variables in a switching period [4-6]. From the average model, a suitable small signal model is then derived by perturbation and linearization around a precise operating point. Finally, the small-signal model is used to derive all the necessary converter transfer functions to design a linear control system by using classical control techniques [7]. The design procedure is well known, but it is generally not easy to account for the wide variation of system parameters, because of the strong dependence of small-signal model parameters on the converter operating point. Multi-loop control techniques, such as current-mode control, have greatly improved power converter dynamic behavior, but the control design remains difficult especially for high-order topologies.

Sliding Mode Control (SMC), which is derived from variable structure system theory, extends the properties of hysteresis control to multivariable environments, resulting in stability even for large supply and load variations, good dynamic response, and simple implementation over the conventional controller. A number of contributions to SMC of power converters with diverse sliding surfaces are available [8-10].

The POELC is a new series of DC-DC converters possessing high-voltage transfer gain, high power density; high efficiency, reduced ripple voltage and current [11]. The voltage lift technique has been successfully employed in the design of DC/DC converters, e.g. three-series luo-converters, in which the output voltage increases stage-by-stage in arithmetic progression [11-12]. However, their circuits are complex. An approach, positive output elementary luo converters, that implements the output voltage increasing in arithmetic progression with a simple structured have been introduced. These converters also effectively enhance the voltage transfer gain. These converters are widely used in computer peripheral equipment, switch mode power supply, medical equipments and also industrial applications, especially for high-voltage projects [11]. Many literatures have reported the general design issues of SMC in dc-dc converters like buck, cuk, and buck–boost converters

[13-14]. Intensive research in the area of DC-DC converter has resulted in novel circuit topologies and these converters in general have complex non-linear models with parameter variation in [15].

Direct regulation/tracking control of the output voltage for POELC results in a non-minimum phase system and therefore an unstable controller. An attempt is made to show that controlling the current can indirectly control the output voltage in converter.

Therefore in this paper, the voltage regulation for POELC operated in CCM using SMC is proposed. The state -space average model for POELC is derived at first and SMC is designed. The detailed discussion of hitting, existence and stability conditions of the SMC for POELC is studied in this paper. The performances of the controller in terms of robustness and dynamic response will be improved by proper selection of the controller gains. Section 2, present the operation and mathematical model of POELC. The design of SMC for POELC is presented in section 3. The design computation of POELC circuit components and the controller gains is well executed in section 4. Simulation results of system at various regions are discussed in section 5. The conclusions and future work of system is discussed in section 6

2. Operations and Mathematical Modeling of POELC

2.1 Operation of POELC

The POELC circuit is shown in Fig. 1. It consists of input dc supply voltage V_{in}, power switch S (N-channel MOSFET), positive luo pump S-L_1-C_1-D and low pass filter L_2-C_2, d duty cycle, load resistance R, V_o average output voltage and I_o average output current.

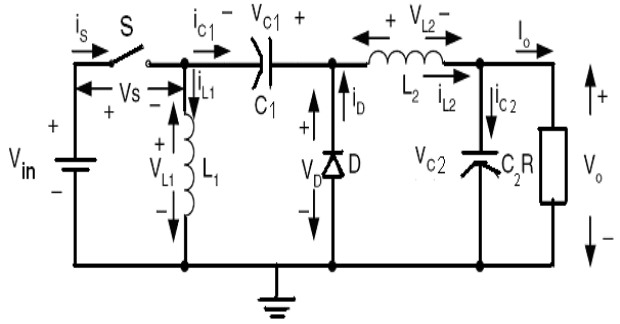

Fig. 1. Circuit diagram of POELC.

In the description of the converter operation, we assume that all the components are ideal and that the POELC operates in a CCM. Figs. 2 and 3 show the two topological modes for a period of POELC operation [11-12].

In mode 1 operation, when the switch is ON, the inductor L_1 is charged by the supply voltage V_{in}. At the same time, the inductor L_2 absorbs the energy from source and the capacitor C_1. The load is supplied by the capacitor C_2. The equivalent circuit of POELC in mode 1 operation is shown in Fig. 2.

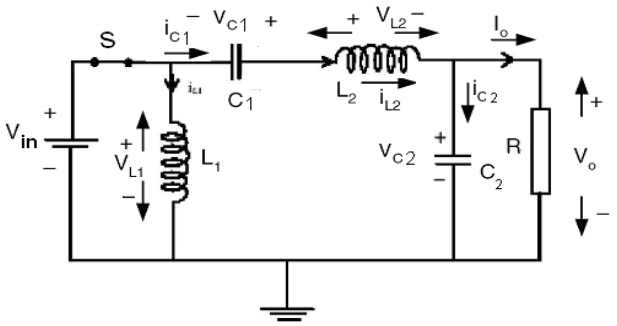

Fig. 2. Equivalent circuit of POELC in Mode 1 operation.

During mode 2 operation, switch is in OFF state, and hence, the current i_{in} drawn from the source becomes zero, as shown in Fig. 3. Current i_{L1} flows through the freewheeling diode D to charge capacitor C_1. Inductor L_1 transfers its stored energy to capacitor C_1. Current i_{L2} flows through the capacitor C_2 and load resistance R, freewheeling diode D to keep itself continuous and both currents i_{L1} and i_{L2} decrease.

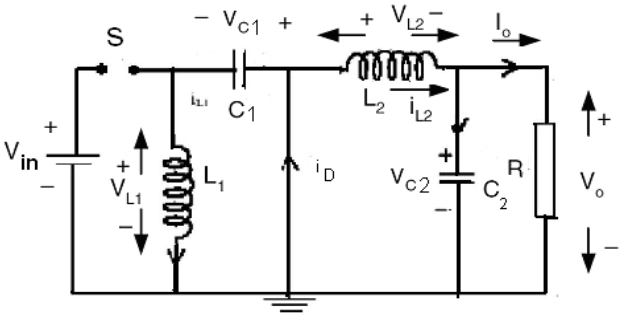

Fig. 3. Equivalent circuit of POELC in Mode 2 operation.

Therefore, the voltage transfer gain of POELC in continuous conduction mode is given by equation (1)

$$G = \frac{V_o}{V_{in}} = \frac{d}{1-d} \tag{1}$$

and the average output current is

$$i_o = \frac{1-d}{d} i_{in} \tag{2}$$

2.2 State Space Averaging Model

The state–space modeling of the equivalent circuit of the positive output elementary luo converter with state variables i_{L1}, V_{C1}, i_{L2} and V_{C2} as follows [16-17]

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{dV_{C1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dV_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L_1} & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_{C1} \\ i_{L2} \\ V_{C2} \end{bmatrix} + \begin{bmatrix} \frac{-V_{C1}+V_{in}}{L_1} \\ \frac{i_{L1}+i_{L2}}{C_1} \\ \frac{-V_{C1}+V_{in}}{L_2} \\ 0 \end{bmatrix} \gamma + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3}$$

$$V_O = \nu_4$$

$$\dot{\nu} = A\nu + B\gamma + C \tag{4}$$

Where γ is the status of the switches, υ and $\dot{\upsilon}$ are the vectors of the state variables (i_{L1}, $V_{C1,}$ $i_{L2,}$ V_{C2}) and their derivatives respectively,

$$\gamma = \begin{cases} 1 \rightarrow S \rightarrow ON \\ 0 \rightarrow S \rightarrow OFF. \end{cases} \tag{5}$$

3. Design of Sliding Mode Controller

In sliding mode theory, the SMC requires sensing of all state variables of POELC and generation of suitable references for each of them [19]. According to principle of the SMC, capacitors voltages V_{C1} and V_{C2} are made to follow as faithfully as possible as to its references. However, the inductor current reference is difficult to evaluate since that generally depends on load power demand supply voltage, and load voltage. To overcome this problem, in implementation the state variable errors for the inductor current (i_{L1} - i_{L1ref}) and (i_{L2} - i_{L2ref}) can be obtained from feedback variable i_{L1} and i_{L2} by means of a high-pass filter in the assumption that their low-frequency component is automatically adapted to actual converter operation. Thus, only the high-frequency component of this variable is needed for the control. This high pass filter increases the system order and can heavily alter the converter dynamics. In order to avoid this problem, the cut-off frequency of the high-pass filter must be suitably lower than the switching frequency to pass the ripple at the switching frequency, but high enough to allow a fast converter response [19].

In the design of the POELC operated in CCM, the following are assumed:

- ideal power switches
- power supply free of dc ripple
- converter operating at high-switching frequency

To require a good output voltage regulation of POELC, the sliding surface equation in the state space, which is expressed by a linear combination of state-variable errors (ε_1, ε_2, ε_3 and ε_4) (respective differences of feedback reference current/voltage and feedback current/voltage)**,** must be selected optimally [18-19].

$$S\left(i_{L1}, V_{C1}, i_{L2} V_{C2}\right) = K_1\varepsilon_1 + K_2\varepsilon_2 + K_3\varepsilon_3 + K_4\varepsilon_4 \tag{6}$$

Where coefficients K_1, K_2, K_3 and K_4 are proper gains, ε_1 is the feedback current error, ε_2 is the feedback voltage error, ε_3 is feedback current error and $\varepsilon_4$is the feedback voltage error, or

$$\varepsilon_1 = i_{L1} - i_{L1ref} \tag{7}$$

$$\varepsilon_2 = V_{C1} - V_{C1ref} \tag{8}$$

$$\varepsilon_3 = i_{L2} - i_{L2ref} \tag{9}$$

$$\varepsilon_4 = V_{C2} - V_{C2ref} \tag{10}$$

$$S\left(i_{L1}, V_{C1}, i_{L2}, V_{C2}\right) = K_1(i_{L1} - i_{L1ref}) + K_2(V_{C1} - V_{C1ref}) + K_3(i_{L2} - i_{L2ref}) + K_4(V_{C2} - V_{C2ref}) \tag{11}$$

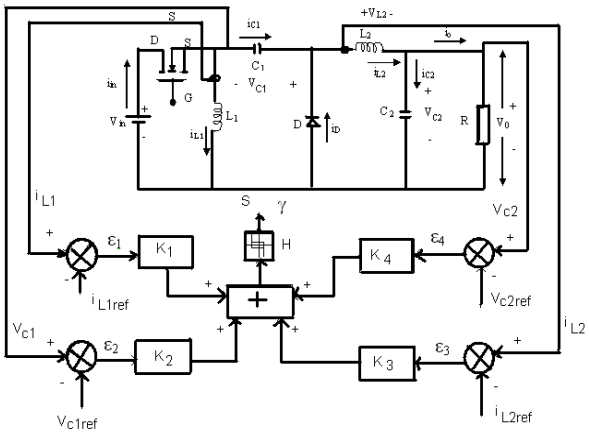

Fig. 4. Principle scheme of SMC applied to POELC.

The signal S (i_{L1}, $V_{C1,}$ $i_{L2,}$ V_{C2}) generated using equation (11) while applied to conventional hysteresis modulator generates the gate pulses to MOSFET switch. The resulted control arrangement is shown in Fig. 4. Status of the switch γ is controlled by hysteresis

block H, which aims to minimize the error of variables i_{L1}, $V_{C1,}$ $i_{L2,}$ and $V_{C2.}$

The system response is determined by the circuit parameters and coefficients K_1, K_2, K_3 and K_4. With a proper selection of these coefficients in any operating condition, high control robustness, stability, and fast response can be achieved.

3.1 Selection of Control Parameters

Once the POELC parameters are selected, inductances L_1 and L_2 and are designed from specified input and output current ripples, capacitors C_1 and C_2 are designed so as to limit the output voltage ripple in the case of fast and large load variations, and maximum switching frequency is selected from the proposed converter ratings and switch type. The system behavior is completely determined by coefficients K_1, K_2, K_3 and $K_{4,}$ which must be selected so as to satisfy existence and ensure stability and fast response, even for large supply variations, load variations, set point variations and also components variations.

According to the variable structure system theory, the converter equations must be written in the following form [18-19]:

$$\dot{x} = Ax + B\gamma + D \tag{12}$$

Where x represents the vector of state-variables errors, given by

$$\dot{x} = \nu - V^* \tag{13}$$

Where $V^* = \left[i_{L1ref}, V_{C1ref}, i_{L2ref}, V_{C2ref} \right]^T$ is the vector of references.

By substituting equation (3) in equation (14), one obtains

$$D = AV^* + C \tag{14}$$

$$D = \begin{bmatrix} 0 & \frac{1}{L_1} & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1ref} \\ V_{C1ref} \\ i_{L2ref} \\ V_{C2ref} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{15a}$$

$$D = \begin{bmatrix} \frac{V_{C1ref}}{L_1} \\ -\frac{i_{L1ref}}{C_1} \\ -\frac{V_{C2ref}}{L_2} \\ \frac{i_{L2ref}}{C_2} - \frac{V_{C2ref}}{RC_2} \end{bmatrix} \tag{15b}$$

Substituting equation (13) in equation (11), the sliding function can be rewritten in the form

$$S(x) = K_1 x_1 + K_2 x_2 + K_3 x_3 + K_4 x_4 = K^T x \tag{16}$$

Where $K^T = \left[K_1, K_2, K_3, K_4 \right]$ and $x = \left[x_1, x_2, x_3, x_4 \right]^T$.

The existence condition of the sliding mode requires that all state trajectories near the surface be directed toward the sliding plane. The controller can enforce the system state to remain near the sliding plane by proper operation of the converter switch.

To make the system state move toward the switching surface, it is necessary and sufficient that [19]

$$\begin{cases} \dot{S}(x) < 0, if\ S(x) > 0 \\ \dot{S}(x) > 0, if\ S(x) < 0 \end{cases} \tag{17}$$

SMC is obtained by means of the following feedback control strategy, which relates to the status of the switch with the value of S(x):

$$\gamma = \begin{cases} 0, for\ S(x) > 0 \\ 1, for\ S(x) < 0. \end{cases} \tag{18}$$

The existence condition equation (17) can be expressed in the form

$$\dot{S}(x) = K^T Ax + K^T D < 0, S(x) > 0 \tag{19}$$

$$\dot{S}(x) = K^T Ax + K^T B + K^T D > 0, S(x) < 0. \tag{20}$$

From a simulation or practical point of view, assuming that error variables x_i are suitably smaller than references V^*, equation (15) and equation (16) can

be rewritten in the form

$$K^T D < 0, S(x) > 0 \tag{21}$$

$$K^T B + K^T D > 0, S(x) < 0. \tag{22}$$

By substituting matrices B and D in equation (20) and equation (21), one obtains

$$\frac{K_1}{L_1}V_{C1ref} - \frac{K_2}{C_1}i_{L1ref} - \frac{K_3}{L_2}V_{C2ref} + \frac{K_4}{RC_2}[i_{L2ref}R - V_{C2ref}] < 0 \tag{23}$$

$$\frac{K_1}{L_1}V_{in} - \frac{K_2}{C_1}i_{L2} + \frac{K_3}{L_2}[V_{in} - V_{C1} - V_{C2ref}] + \frac{K_4}{RC_2}[i_{L2ref}R - V_{C2ref}] > 0 \tag{24}$$

The existence condition is satisfied if the inequalities equation (21) and equation (22) are true.

Finally, it is necessary to guarantee that the designed sliding plane is reached for all initial states. If the sliding mode exists, in the system defined by equation (6), it is a sufficient condition that coefficients K_1, K_2, K_3 and K_4 be nonnegative.

3.2 Switching Frequency

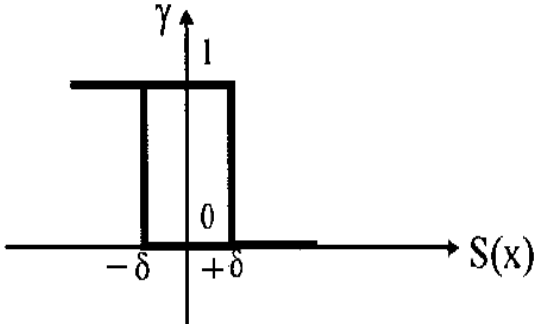

Fig.5. Switching function γ.

In the ideal sliding mode at infinite switching frequency, state trajectories are directed toward the sliding surface and move exactly along it. A practical system cannot switch at infinite frequency. Therefore, a typical control circuit features a practical relay, as indicated in Fig. 5. A practical relay always exhibits hysteresis modeled by

$$\gamma(s) = \begin{cases} 0, & when\ \ S > +\delta\ or \\ & when\ \dot{S} < 0 and\ |S| < \delta \\ 1, & when S < -\delta or \\ & when\ \dot{S} > 0 and\ |S| < \delta \end{cases} \tag{25}$$

Where δ is an arbitrarily small positive quantity and 2δ is the amount of hysteresis in S(x). The hysteresis characteristic makes it impossible to switch the control on the surface S(x) = 0. As a consequence, switching occurs on the lines S =± δ, with a frequency depending on the slopes of i_{L1} and i_{L2}. This hysteresis causes phase plane trajectory oscillations of width 2δ, around the surface S(x) = 0 as shown in Fig. 6. Note that Fig. 5 simply tells us that in Δt_1 function S(x) must increase from (–δ to δ) ($\dot{S} > 0$), while in Δt_2 function $S(x)$ must decrease from +δ to δ ($\dot{S}$ <0).

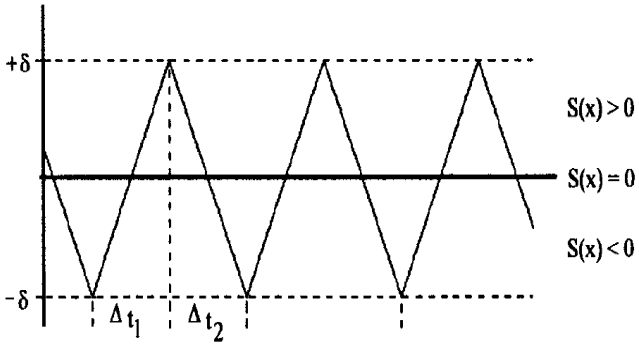

Fig. 6. The waveform of S(x).

The switching frequency equation is obtained from Fig.6, by considering that the state trajectory is invariable, near to the sliding surface S(x) = 0 and is given by

$$f_s = \frac{1}{\Delta t_1 + \Delta t_2} \tag{26}$$

Where Δt_1 is conduction time of the switch S and Δt_2 is the off time of the switch S. The conduction time Δt_1 is derived from equation (24) and it is given by

$$\Delta t_1 = \frac{2\delta}{\frac{K_1}{L_1}V_{in} - \frac{K_2}{C_1}i_{L2} + \frac{K_3}{L_2}[V_{in} - V_{C1} - V_{C2ref}] + \frac{K_4}{RC_2}[i_{L2ref}R - V_{C2ref}]} \tag{27}$$

The off time Δt_2 is derived from equation (23), and it is given by

$$\Delta t_2 = \frac{-2\delta}{\frac{K_1}{L_1}V_{C1ref} - \frac{K_2}{C_1}i_{L1ref} - \frac{K_3}{L_2}V_{C2ref} + \frac{K_4}{RC_2}[i_{L2ref}R - V_{C2ref}]} \quad (28)$$

The maximum switching frequency is obtained substituting equation (27) and equation (28) in equation (26) in the assumption that the converter is operating with non-load ($i_{L1ref} = 0$, $i_{L2ref} = 0$ and $1/R = 0$) and the output voltage reference is passing by maximum $V_{C1ref\,(max)}$ and $V_{C2ref(\,max\,)}$. The maximum switching frequency is obtained as equation (29)

$$f_{s(\max)} = \frac{K_1 K_3 V_{in}}{2\delta L_1 L_2}\left(1 - \frac{V_{in}}{V_{C1ref(\max)} + V_{C2ref(\max)}}\right) \quad (29)$$

3.3 Duty Cycle

The duty cycle d(t) is defined by the ratio between the conduction time of the switch S and the switch period time, as represented by

$$d(t) = \frac{\Delta t_1}{\Delta t_1 + \Delta t_2} \quad (30)$$

Considering the sliding mode control an instantaneous control, the ratio between the output and the input voltages must satisfy in any working condition.

$$\frac{V_O}{V_{in}} = \frac{1}{1 - d(t)} \quad (31)$$

3.4 Inductor Currents

The high- frequency or maximum inductor current ripple is obtained from Fig. 2 and given by [15]

$$\Delta_{L1} = \frac{\Delta t_1 V_{in}}{L_1} \quad (32)$$

$$\Delta_{L2} = \frac{\Delta t_1 V_{in}}{L_2} \quad (33)$$

3.5 Capacitor Voltages

The controller operates over the switch to make the capacitors voltage V_{C1} (t) and V_{C2} (t) follow its reference. Over V_{C1}(t) and V_{C2}(t), a high-frequency ripple (switching) is imposed, which is given by [15]

$$\Delta Vc_1(t) = \frac{V_{C1}}{RC_1}\Delta t_1 \quad (34)$$

$$\Delta Vc_2(t) = \frac{V_{C2}}{RC_2}\Delta t_1. \quad (35)$$

It is interesting to note that the switching frequency, inductor current ripple, and capacitor voltage ripple depend on the following terms: the control parameters, circuit parameters, reference voltage, output capacitor voltage V_{C2}(t), pump capacitor voltage V_{C1}(t), and inductor currents i_{L1}, i_{L2}.

It is important to determine the circuit parameters and coefficients K_1, K_2, K_3 and K_4 that agree with desirable values of maximum inductor current ripple, maximum capacitor voltage ripple, maximum switching frequency, stability, and fast response for any operating condition.

4. Design Computation of Circuit Components and Controller Parameters

The main purpose of this section is to use the previously deduced equations to calculate the POELC components value and controllers' parameters.

4.1 Calculation of V_{C2}

From equation (28) and a simulation point of view, the output voltage is chosen to produce a duty cycle close to 0.75. The adopted value of the output voltage V_o is 36 which is in Table 1, and a variation of the duty cycle between $d_{min} = 0.4$ and $d_{max} = 0.9$ is expected. Finally $V_{C2max} = 108$V.

4.2 Determination of Ratio K_1 / L_1 and K_3 / L_2

Substituting V_{in}, $V_{C2ref} = V_{C2max}$, and δ=0.75 in equation (29), the value of K_1 / L_1 and K_3 / L_2 is obtained as K_1 / L_1 and $K_3 / L_2 = 15000$. There are some degrees of freedom in choosing the ratio K_1 / L_1 and K_3 / L_2. It is recommendable to choose the ratio K_1 / L_1 and K_3 / L_2 to agree with required levels of stability and response speed. The final adopted value is, K_1 / L_1 and $K_3 / L_2 = 1200$.

4.3 Determination of Ratio K_2 / C_1 and K_4 / C_2

From equation (23) and equation (24) and taking $i_{L1ref} = i_{L1(max)} = 2.16$A and $i_{L2ref} = i_{L2(max)} = 2.3$A, one obtains $12008 < K_2 / C_1 < 2848433$ and $12008 < K_4$

$/ C_2 < 2848433$.

There are some degrees of freedom in choosing the ratio K_2 / C_1 and K_4 / C_2**.** In this controller, the ratio K_2 / C_1 and K_4 / C_2 is a tuning parameter. It is recommendable to choose the ratio K_2/C to agree with required levels of stability and response speed. The ratio K_2 / C_1 and K_4 / C_2 is chosen by iterative procedure (i.e. the ratio is modified until the transient response is satisfactory), and it is verified by simulation. The final adopted value is, K_2 / C_1 = and K_4 / C_2=40000.

4.4 Calculation of L_1 and L_2

The maximum inductor current ripple is chosen to be equal to 15% of maximum inductors current and the inductors value which is obtained from equation (32) and Eq. (33) as L_1 and L_2 =1mH.

4.5 Calculation of C_1 and C_2

The maximum capacitor ripple voltage ΔV_{c1max} and ΔV_{c2max} is chosen to be equal to 1% maximum capacitors voltage and capacitors C_1 and C_2 are determined using equation (34) and equation (35) as 20μF.

4.6 Values of the Coefficients K_1, K_2 , K_3 and K_4

Having decided on the values of the ratio K_1 / L_1 and K_3 / L_2 inductor, the value of K_1 and K_3 is unswervingly obtained (K_1=1.2 and K_3=1.2). Similarly the K_2 and K_4 (K_2 = 0.8 and K_4=0.8) is computed using the ratio K_2 / C_1 and K_4 / C_2 and capacitors C_1 and C_2.

5. Simulation Study

The main purpose of this section to discusse about the simulation studies of the POELC with designed SMC. The validation of the system performance is done for five regions viz. transient region, line variations, load variations, steady state region and also components variations. The simulations have been performed on the POELC circuit with parameters listed in **Table 1**.

The static and dynamic performances of SMC for POELC are evaluated in MatLab/Simulink software platform. The detailed operation of SMC for POELC is presented in sections 2 and 3.

Table 1
Parameters of the POELC.

Parameters name	Symbol	Value
Voltage	Vin	12V
Output Voltage	Vo	36V
Inductors	L_1, L_2	1mH
Capacitors	C_1, C_2	20 μF
Nominal switching frequency	Fs	100kHz
Load resistance	R	50Ω
Output power	Po	25.92W
Input power	Pin	25.92W
Input current	Iin	2.16A
Range of duty ratio	d	0.4 to 0.9
Adopted value of duty ratio	d	0.75

5.1 Transient Region

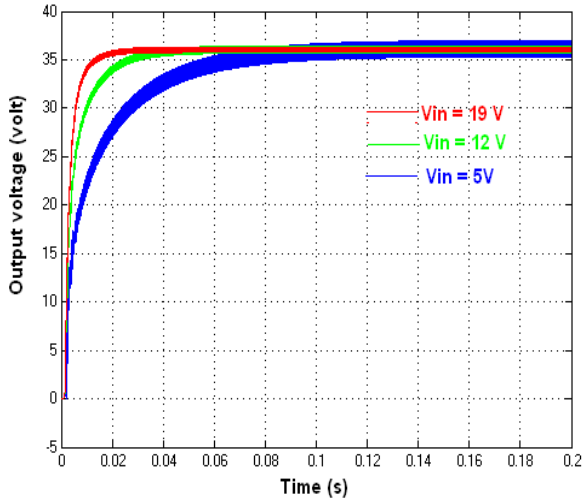

Fig. 7. Response of output voltage of POELC in startup for various input voltage.

Fig. 7 shows the dynamic behavior in the startup for output voltage of POELC for different input voltage like 5V, 12V and 19V respectively. It can be seen that output voltage of POELC for Vin = 5 V, 12 V, and 19 V has negligible overshoot and settling times of 0.1 s, 0.04 s and 0.02 s in startup with designed SMC.

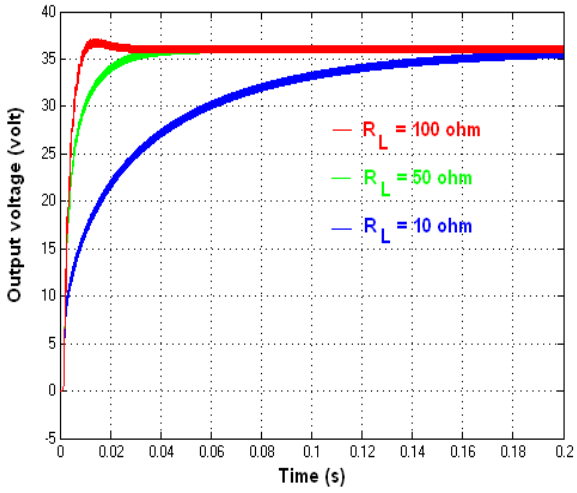

Fig. 8. Response of output voltage of POELC in startup for various load resistances.

Fig. 8 shows the dynamic behavior in the startup for output voltage of POELC for various load resistances like 10 Ω, 50 Ω, and 90 Ω respectively. It can be seen that output voltage of POELC has slightly overshoot and settling time of 0.028 s for R = 100 Ω, where as the output voltage of POELC for R = 50 Ω and 90 Ω has negligible overshoot and settling times of 0.03 s and 0.17 s in startup with designed SMC.

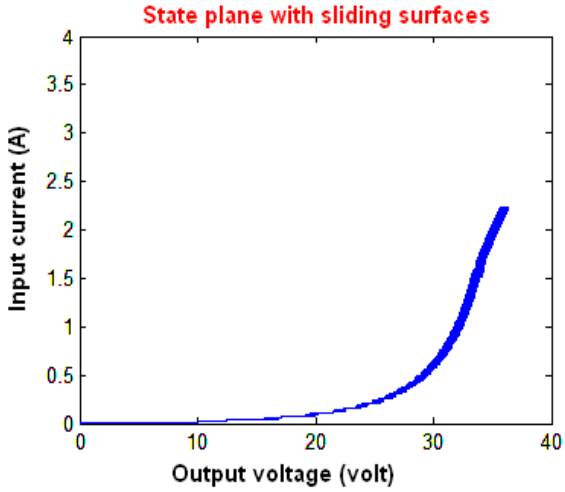

Fig. 9. System startup in the state plane with sliding faces.

Fig. 9 represents a simulation of the dynamic behavior in the state plane for the input current and output voltage of POELC with designed SMC in sliding surfaces. It can be found that input current of POELC goes up to 2.16 A and output voltage of POELC travels up to 36 V without overshoot.

5.2 Line Variations

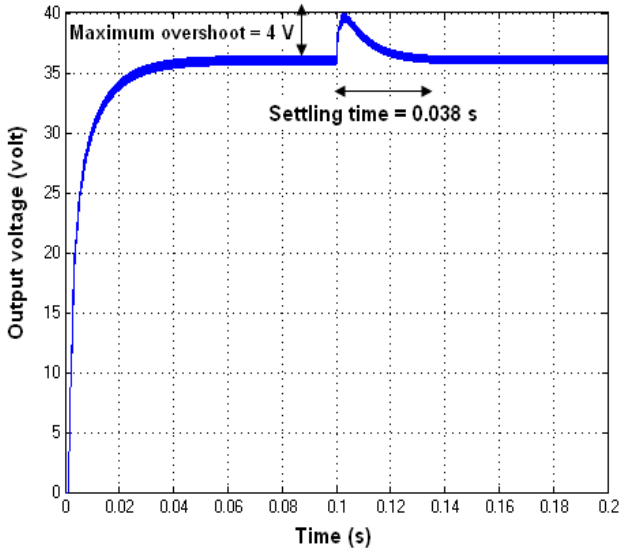

Fig. 10. Response of output voltage of POELC for input step change from 12V to 15 V.

Fig. 10 shows the response of average output voltage of POELC for input voltage step change from 12 V to 15 V (+30% line variations). It can be found that the output voltage of POELC has maximum overshoot of 4

V and settling time of 0.038 s with designed SMC.

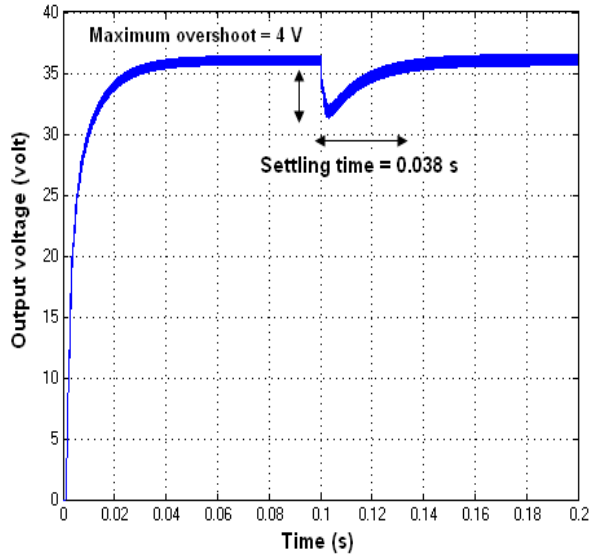

Fig. 11. Response of output voltage of POELC for input step change from 12V to 9V.

Fig. 11 shows the response of average output voltage of POELC for input voltage step change from 12 V to 9 V (-30% line variations). It can be found that the output voltage of POELC has maximum overshoot of 4 V and settling time of 0.038 s with designed SMC.

5.3 Load Variations

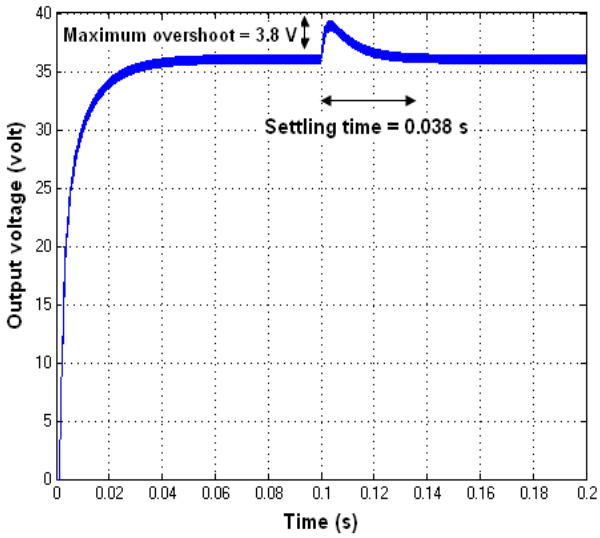

Fig. 12. Response of output voltage of POELC when load value takes a step changes from 50 Ω to 60 Ω.

Fig. 12 shows the response of output voltage of POELC for load step change 50 Ω to 60 Ω (+20% load variations). It could be seen that the output voltage of POELC has maximum overshoot of 3.8 V and settling time of 0.038 s with proposed control scheme.

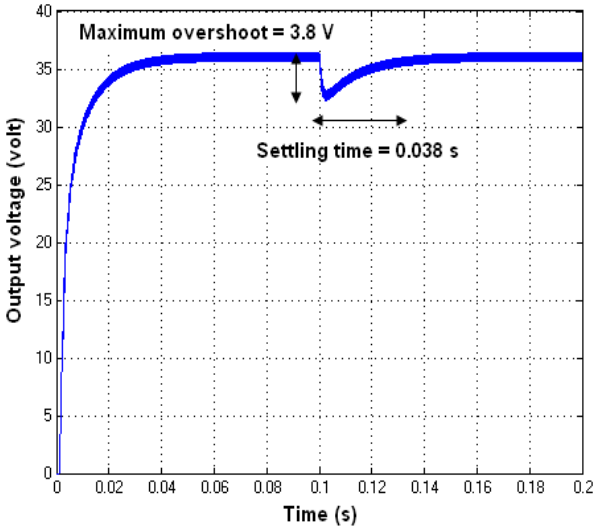

Fig. 13. Response of output voltage of POELC when load value takes a step changes from 50 Ω to 40Ω.

Fig. 13 shows the response of output voltage of POELC for load step change 50 Ω to 40 Ω (-20% load variations). It could be seen that the output voltage of POELC has maximum overshoot of 3.8 V and settling time of 0.038 s with proposed control scheme.

5.4 Steady State Region

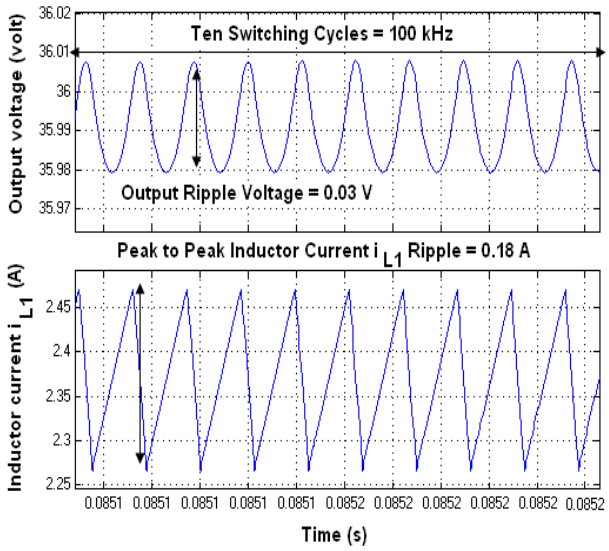

Fig. 14. Response of output voltage and inductor current i_{L1} in steady state condition.

Fig. 14 shows the instantaneous output voltage and inductor current i_{L1} of POELC with proposed control scheme in steady state region. It is evident from the figure that the output voltage ripple is very small 0.03V and peak-to-peak inductor current ripple is 0.18 A for the average switching frequency (100 kHz) closer to theoretical designed value listed in **Table 1**.

5.5 Components Variation

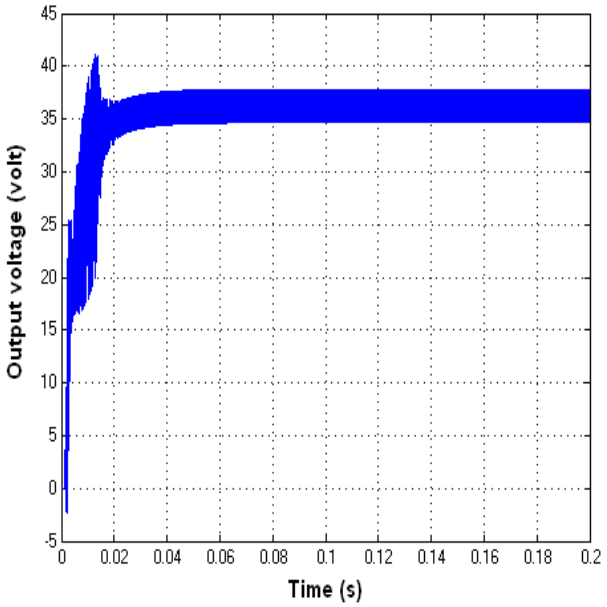

Fig. 15. Output voltage when inductors (L_1 & L_2) variation from 1mH to 2mH.

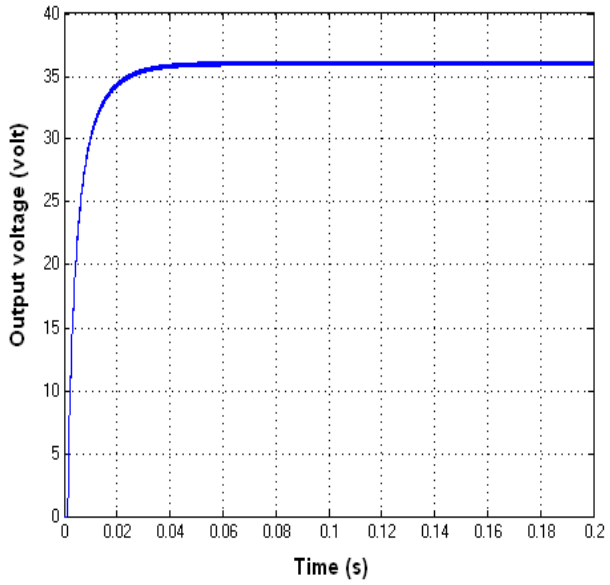

Fig. 16. Output voltage when capacitors (C_1 & C_2) variation from 20 µF to 50 µF.

Fig. 15 shows the output voltage of POELC with proposed control scheme for inductor variation from 1mH to 2mH. It could be found that the change does not influence the converter behaviour due to proficient design of SMC.

An interesting result is illustrated in Fig. 16. It shows the output voltage response of POELC with proposed control scheme for the variation in capacitor values 20µF to 50µF. It can be seen that the SMC is very successful in suppressing effect of capacitance variation except that a negligible output voltage ripples.

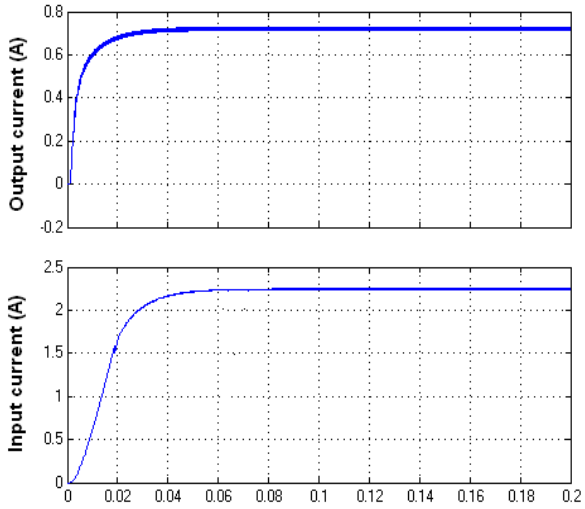

Fig. 17. Average input and output current of POELC.

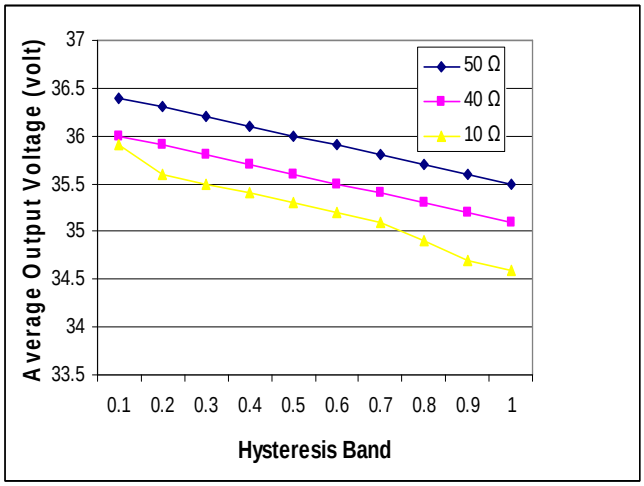

Fig. 18. Simulated measured average output voltage of POELC at Vin =12 V and load R = 10 Ω, 40 Ω and 50 Ω for different hysteresis band settings.

Fig.17 shows the average input current and output current of POELC with proposed control scheme respectively. It is showed that the average input current is 2.16A and average output current is 0.72A, which is very closer to theoretical value in **Table 1**. Using simulation analysis the POELC with hysteresis rule based SMC computes that the input and output power values are 25.92W and 25.92W respectively, which is very closer to the calculated theoretical value listed in **Table 1**.

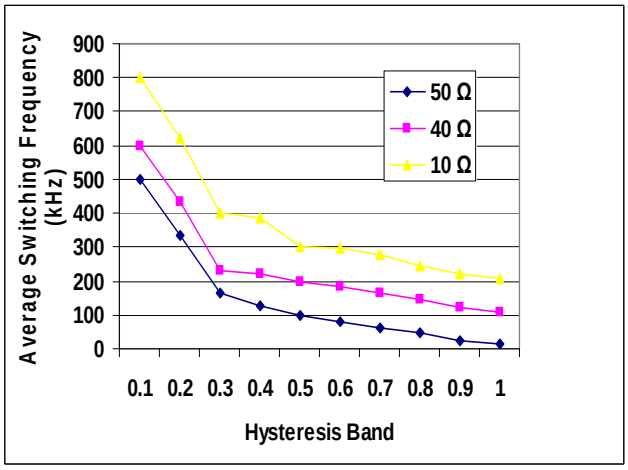

Fig. 19. Simulated measured average switching frequency of POELC at Vin = 12 V and load R= 10 Ω, 40 Ω and 50 Ω for different hysteresis band settings.

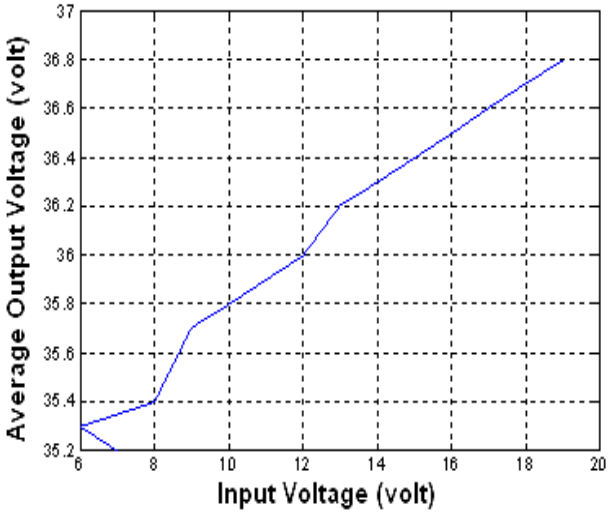

Fig. 20. Simulated measured average output voltage of POELC for different input voltage.

Figs. 18 and 19 shows the graphs of simulated measured average output voltage and average switching frequency of POELC against hysteresis band for load resistances R = 10 Ω, 40 Ω, and 50 Ω respectively. From the figure, the average output voltage is lower with lower load resistance, and average switching frequency is notably higher with lower load resistance with designed SMC.

The simulated measured average output voltage of POELC for input voltage range 6V to 19V is plotted in Fig. 20. It can be found that the average output voltage increase with increasing input voltage with designed SMC. Specifically, output voltage deviation of POELC is 0.1 V for the entire input voltage range.

A Proportional-Integral (PI) controller with settings K_p = 0.0112 and T_i = 0.0113s obtained by the Ziegler-Nichols tuning technique [20] has been used for comparison with the designed SMC. Figs. 21 and 22 show the simulated time domain performances evaluation of current/voltage profiles of POELC using SMC versus PI controller. From this figures it is clearly identified that the simulated results of the designed SMC are showed better performance over the PI controller under line and load disturbances in steady state operating region.

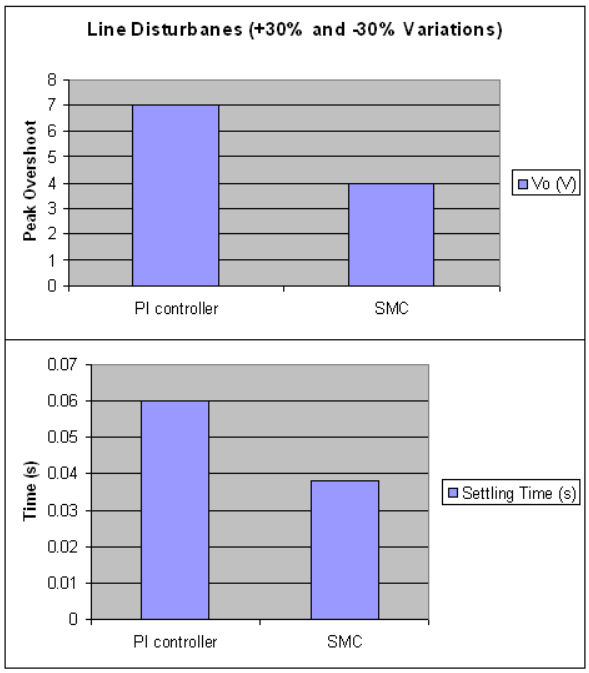

Fig.21. Time domain performances evaluation of POELC using SMC versus PI controller under line disturbances in steady state operating region.

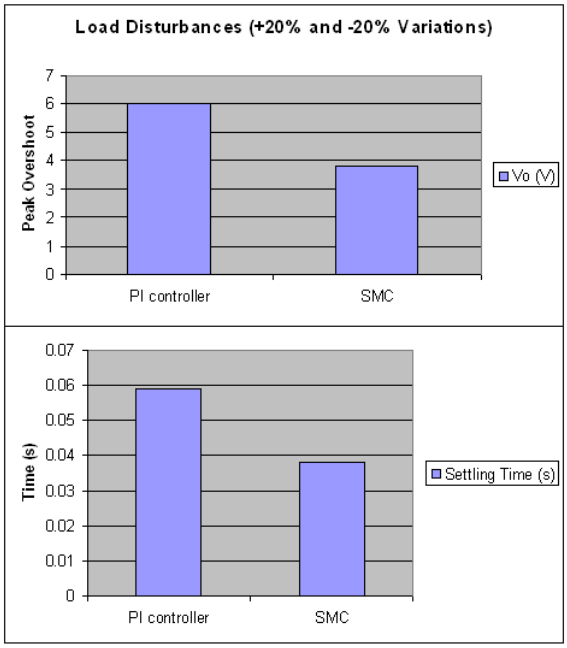

Fig.22. Time domain performances evaluation of POELC using SMC versus PI controller under load disturbances in steady state operating region.

6. Conclusions

Switched mode DC-DC power converters are used in variety of electric power supply systems, including cars, ships, aircrafts, high voltage projects and computers. Power electronic converters are intrinsically periodic time-variant structure systems due to their inherent switching operation, so the sliding mode control approach is a strong candidate method for the converter controller design.

The design and output voltage regulation of SMC for POELC operated in CCM has been successfully demonstrated in this paper. A SMC over the output capacitor voltage and inductor current has been used for the control. The influence of the control parameters on the performances of the system was studied. The effect of proper selected controller parameters of sliding mode controlled POELC operated in CCM resulted in fast dynamic response and excellent static and transient responses over the conventional controller. It is, therefore, feasible for common DC-DC conversion purpose, computer power supplies and medical equipments etc. Further research may focus to the study the experimental set-up of the proposed system.

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Biography

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Dr.S.Jeevananthan was born in Nagercoil, India on May 25, 1977. He received the B.E. degree in Electrical and Electronics Engineering from MEPCO SCHLENK Engineering College, Sivakasi, India, in 1998, and the M.E. degree from PSG College of Technology, Coimbatore, India, in 2000. He completed his Ph.D. degree from Pondicherry University in 2007. Since 2001, he has been with the Department of Electrical and Electronics Engineering, Pondicherry Engineering College, Pondicherry, India, where he is an Assistant professor.

He has made a significant contribution to the PWM theory through his publications and has developed close ties with the international research community in the area. He has authored more than 50 papers published in international and national conference proceedings and professional journals. Dr.S.Jeevananthan regularly reviews papers for all major IEEE TRANSACTIONS in his area and AMSE periodicals (France). He is an active member of the professional societies, IE (India), MISTE, SEMCE, and SSI.