Abstract: This article presents a novel negative output elementary super lift Luo converter (NOESLLC) based on the Sheppard-Taylor (S-T) topology operated in a continuous inductor current with the classical proportional-integral (PI) controller for high voltage applications. The NOESLLC based on S-T is one of the topologies of DC choppers. The advantages of NOESLLC based on S-T over the traditional NOESLLCs are reduced ripples in the inductor current and capacitor voltage, high output voltage generation with minimum duty ratio, high voltage transfer gain, and a simpler structure. The NOESLLC based on S-T is built with fewer components and devices compared to the S-T converter and the conventional NOESLLC. Further, it is capable of manipulating the output voltage and produces good efficiencies at different operating stages through different input voltages, load resistances, and duty cycles. The importance of NOESLLC based on S-T over the traditional soft switching converters is that its main switches close with Zero Current Switching (ZCS) and the diodes open with Zero Voltage Switching (ZVS). In this study, the classic PI controller was designed for NOESLLC on the basis of S-T to improve its dynamic performance and output voltage regulation for different supply voltages and load resistance variations. The characteristics of the NOESLLC based on S-T using a classical PI controller are verified through a MATLAB/Simulink model under different working conditions compared with the traditional NOESLLC. The results show that the NOESLLC based on S-T is more capable in comparison with the conventional NOESLLC.

Keyword: Super lift Luo-converter, negative output super lift Luo-Converter, sheppard taylor, continuous conduction mode, soft-switching, zero transition switching, classical PI controller and state-space average modeling.

NOMENCLATURE

- $V_{in}$: Input voltage
- $C_1$, $C_2$ and $C_3$: Energy storage Capacitors
- $L$: Inductor
- $V_L$: Voltage across the inductor
- $D_1$, $D_2$, $D_3$, $D_4$: Diodes
- $V_{c1}$: Voltage across the capacitor one
- $V_o$: Output voltage
- $d$, $d_1$: Duty ratio
- $T$: Switching time period
- $V_{c3}$: Voltage across the capacitor 3
- $L_B$: Critical inductance
- $i_L$: Inductor current
- $i_o$: Output current
- $V_{c2}$: Voltage across the capacitor 2
- $I_{in}$: Input current
- $P_o$: Output power
- $P_{in}$: Input power
- $i_{LB}$: Inductor current at boundary
- $R$: Load resistance
- $R_B$: Boundary load resistance
- $T_B$: Switching time period at boundary
- $S_1$ and $S_2$: Switches

I. INTRODUCTION

Recently, the switching mode power supplies and regulators have been used extensively over the traditional linear power supplies as they have good efficiency, are compact and light weight, cost effective and work on smaller power ratings (about 28 W). In recent times, DC-DC converters have played a major role in commercial applications such as mobile phones, medical equipment, computer hardware parts, robot systems, LED TVs, and military applications [1].
The Sheppard-Taylor (S-T) converter is commonly used to generate non-pulsating input/output currents analogous to the C’uk converter [2]. The S-T topology is examined as a possible development topology of the C’uk topology. The direction of power flow in a C’uk converter circuit is bi-directional, whereas the S-T topology circuit operates uni-directionally.

The S-T converter consists of dual storage coils that can shape the input current and feed the output load thereby reducing the input and output current ripples. It is capable of regulating the output voltage while the input voltage and load resistance are modified. The S-T converter can regulate the output voltage more efficiently due to an insensitive input resistance compared to the C’uk converter. Therefore, it is better suited for power factor correction (PFC) applications [3]. In general, the S-T converter structure consists of 4 diodes and 2 power switches working in synchronization. Further, the lack of synchronization between the 2 switches does not lead to converter break down. A drawback of the S-T converter is the nominal ON/OFF power loss particularly when the converter operates at higher frequencies.

A lot of investigations on PFC applications based on the S-T converter have been reported in the surveys [4-10]. Yet, not a large amount of improvement on S-T topology has been reported [7-9]. The new boost DC-DC converters based on the S-T has been reported [11]. The key merits of boost converter based on S-T are capable of regulating the output voltage during a wide range of input voltage or load variations, constructed with fewer components compared with the normal S-T converter topology. Main switches of this converter are closed with Zero-Current-Switching (ZCS), and the rectifier diodes are open with Zero-Voltage-Switching (ZVS). The negligible input current ripple of this converter makes the input filter not essential and works at lower duty ratio.

Considerable work has been done on the applications of PFC based on the S-T converter [4-10]; however, there are not many studies available on the improvements of S-T topology [7-9]. Studies on the new boost DC-DC converters based on S-T are well accomplished [11] with key merits being the capability of manipulating the output voltage in input voltage and load resistance variations and having fewer components compared with the traditional S-T converter topology. In this converter, Zero-Current-Switching (ZCS) is achieved by turning on the main switches whereas the Zero-Voltage-Switching (ZVS) is obtained by turning off the diodes. The converter does not require an input filter due to a small amount of input current ripple and works on lower duty ratio.

Luo converters (LCs) belong to a new class of DC-DC converters which originate from the basic DC-DC converters employing voltage lift techniques (VLT) [12]. The merits of LCs over the traditional DC-DC converters are excellent voltage transfer gain, increased power density, good efficiency, output capacitor voltage, and inductor current with lesser ripples, economical topology, simple structure, and getting rid of parasitic elements [13-15]. The negative output elementary super lift Luo converter (NOESLLC) [16] is one of the topologies of LCs. In this article, the NOESLLC is considered for S-T study with classical Proportional-Integral (PI) controller. The PI controller for double output elementary Luo converter was presented in [17]. The output voltage response of the converter with designed PI controller produces more peak overshoots, about 15V, for the line and load disturbances.

A series of negative output VLT-C’uk converters have been developed [18]. The step-up DC-DC converter with the coupled inductor and VLT was studied [19]. However, it creates good voltage transfer gain with a complex structure. The general modeling and design of the Sliding Mode Controller (SMC) for triple lift LC using Super Lift Technique (SLT) have been well accomplished [20]. The ZVS-QR based elementary circuit of VLT and SLT converters using an analog controller UC 3861 was proposed earlier [21-22]. However, with this controller, the efficiency of these converters came to be 91%.

The classical PI controller for positive output super lift converter with PV system has been studied [23]. Its start-up region has been found to produce maximum overshoots of around 16V. The modeling and simulation of KY voltage boost converter with a direct method of sliding mode controller (SMC) were carried out [24]. This design control method produced peak overshoots of 4V and 1V respectively for in line and load variations. A complete study of the negative output KY boost converter with the classical linear proportional-integral (PI) controller was carried out [25], and huge overshoots and longer settling times were reported. The SMC with the intelligent controller for positive output elementary split inductor type boost converter has been studied [26]. Until now, this controller has produced good characteristics during various stages. The SMC along with proportional dual integral controller for negative output super lift converters have been studied [27-30]. The design
controlled technique for these converters produced more peak overshoot and ripples in the capacitor voltage.

From the available literature, it is clear that NOESLLC based on S-T has not been studied so far. Hence in this article, a NOESLLC based on S-T operated in CCM using a classical PI controller has been proposed. The state space equations of this converter were derived and the classical PI controller parameters were determined. The performance of NOESLLC based on S-T using PI controller was validated under different operating conditions via a MATLAB/Simulink model compared to the traditional NOESLLC.

II. THE CONSTRUCTION AND ANALYSIS OF NOESLLC BASED ON S-T

The NOESLLC based on S-T is shown in Fig. 1 (a). It consists of two power switches (S₁ and S₂), four diodes (D₁, D₂, D₃, D₄), one inductor L, three capacitors (C₁, C₂, C₃), an input voltage Vᵢn, and a load resistance R. The inductor current is kept constant at all times by choosing large values for L, C₂, and C₃. The operation of NOESLLC based on S-T consists of three modes, illustrated in Fig. 1.

In Mode 1 (see Fig. 1b), S₁ and S₂ are closed, C₁ is de-energized, D₁, D₂, and D₄ are open and D₃ is closed. The inductor current rises linearly as \((Vᵢn + V_c₁)\). The input source and C₁ dispense energy to L. At the beginning of Mode 1, the voltage of C₁ is \((Vᵢn - V_L)\), thus the energy in C₁ is \(C₁(Vᵢn - V_L)²/2\).

In Mode 2 (see Fig. 1c), S₁ and S₂ are open, D₃ is closed and D₄ is open while \(V_c₁\) is less than \(V_o\). C₁ is energized to help the source and the inductor through D₁ and D₂, and the inductor current \(i_L\) falls.

In Mode 3 (see Fig. 1d), while \(V_c₁\) is more than \(V_o\), D₄ conducts since \(V_c₁\) is less than the \(V_o\). The input supply and inductor provide power to the load R.

The analysis of the designed converter (Fig. 1a) was performed by making the following assumptions:

- The NOESLLC based on S-T works in a constant state,
- The current in the coil is continuous,
- The capacitor size is large and a constant voltage \(V_o\) is maintained,
- The switches are ON for a period \(dT\) and OFF for period \((1-dT)\)

- The circuit elements are ideal.
A. Mode 1 Operation Analysis

In Mode 1 (Fig. 1b), $S_1$ and $S_2$ are closed and $V_L$ is derived from the Kirchhoff's Voltage Law (KVL).

\[
V_L = V_{in} + V_{c1} \\
\frac{di_L}{dt} = \frac{V_{in} + V_{c1}}{L} \\
V_{c3} = V_o
\]

While $\frac{di}{dt}$ is a positive constant, the current rises linearly and is expressed as

\[
(Ai_L)_{closed} = \left( \frac{V_{in} + V_{c1}}{L} \right) dT
\]

B. Mode 2 Operation Analysis

In Mode 2 (refer the Fig. 1c), the switches $S_1$ and $S_2$ are open, and the $D_4$ is open, since $V_{c1} < V_o$. The $C_1$ is charged by the source and the inductor. The voltage across the inductor $V_L$ is expressed as

\[
V_L = V_{in} - V_{c1} \\
\frac{di_L}{dt} = \frac{V_{in} - V_{c1}}{L} \\
V_{c3} = V_o
\]

While, the $\frac{di}{dt}$ is a negative constant, the current is fall linearly as shown in Fig. 1c and it is written as

\[
(Ai_L)_{open} = \left( \frac{V_{in} - V_{c1}}{L} \right) \left( 1 - dT \right)
\]

For steady-state working, the $i_L$ at the end of the T is the same as that at the start, which means that the net change in $i_L$ over one complete period is null

\[
(Ai_L)_{closed} + (Ai_L)_{open} = 0
\]

Substituting (2) and (4) in (5) becomes

\[
(V_{in} + V_{c1}) dT + (V_{in} - V_{c1}) (1 - dT) = 0
\]

\[
V_{c1} = \frac{V_{in}}{1-2d}
\]

C. Mode 3 Operation Analysis

In Mode 3 (see Fig. 1d), $S_1$ and $S_2$ are open and $D_4$ is closed. Prior to Mode 3, the $V_{c3}$ reduces due to freewheeling. At the end of Mode 2 ($t=d_1T$), $C_1$ continues to be energized, the diode $D_4$ conducts when $V_{c1}=V_o$ and $V_{c3}$ is clamped at $V_{in}$ (the corresponding circuit is shown in Fig. 1d). At $t=d_1T$, $V_{c1}=V_{c3}=V_o$ and the capacitor voltages are specified by

At ($t=dT$)

\[
V_{c1}(dT)=\frac{-1}{C_1} \int_{0}^{dT} i_L dt + V_{c1}(dT) \\
V_{c1}(dT)=\frac{-1}{C_1} i_L (dT) + V_{c1}(0)
\]

Substituting (7) into (8)

\[
V_{c3}(dT)=\frac{1}{C_1} \int_{0}^{dT} i_L dt + V_{c1}(dT) \\
V_{c3}(dT)=\frac{1}{C_1} i_L (d_1-d)T + V_{c1}(0)
\]

Similarly,

\[
V_{c3}(dT)=\frac{-1}{C_3} \int_{0}^{dT} i_o dt + V_{c3}(0) \\
V_{c3}(dT)=\frac{-1}{C_3} i_o d_1T + V_{c3}(0)
\]

Let, $V_1=V_{c3}$, we solve for $d_1$
\[
\frac{1}{C_i} i_L (d_1 - 2d) T + V_{c1}(0) = \frac{1}{C_3} - i_o d_i T + V_{c3}(0)
\]
\[
\frac{1}{C_i} i_L (d_1 - 2d) T = \frac{1}{C_3} i_o d_i T
\]
(11)

By applying the power balance condition and it is expressed as (12)
\[
P_{in} = P_o = V_{in} i_L = V_o i_o
\]
(12)

Simplifying the (12) and then
\[
i_o = (1-2d)i_L
\]
(13)

Substituting (13) into (11)
\[
\frac{1}{C_i} i_L (d_1 - 2d) T = \frac{1}{C_3} (1-2d)i_L d_i T
\]
\[
d_1 = \frac{2C_3 d}{C_3 + C_1 (1-2d)} \quad V_o = V_{c1} = \frac{V_{in}}{1-2d}
\]
(14)

**D. Critical Inductance Analysis**

The critical inductance \( L_B \) (B indicates the boundary) is bounded between the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM). The average value of the inductor current at the boundary \( i_{LB} \) is
\[
i_{LB} = \frac{1}{2} \Delta i_L
\]
(15)

Owing to
\[
\Delta i_L = \frac{V_{in} + V_{c1}}{L} dT = \frac{V_{in} - V_{c1}}{L} (1-d) T
\]
(16)

Substituting (16) into (15)
\[
i_{LB} = \frac{V_{in} + V_{c1}}{2L} dT = \frac{(1-2d)V_{c1} - V_{c1}}{2L} dT
\]
\[
= \frac{V_o}{L} (1-d) dT
\]
(17)

Therefore, if the average output current is smaller than \( i_{LB} \), given by (17), then \( i_i \) will become discontinuous.

\[
i_{ob} = i_{LB} (1-2d) = \frac{V_v}{L} d(1-d)(1-2d)
\]
(18)

From (18), the required \( L \) to ensure a CCM of the NOESLLC based on S-T is
\[
L \geq L_B = \frac{V_v}{I_{oB}} d(1-d)(1-2d) = d(1-d)(1-2d)RT
\]
(19)

\[
R \geq R_B = \frac{V_v}{I_{oB}} = \frac{L}{d(1-d)(1-2d)T}
\]
(20)

\[
T \geq T_B = \frac{L}{d(1-d)(1-2d)R}
\]
(21)

**E. Output Ripple Voltage Analysis**

The above-deduced equations are derived with the assumption that \( V_o \) is kept fixed. In real-time executions, instabilities in \( V_o \) or the voltage ripples always exist. The \( \Delta V_o \) can be evaluated from the capacitor current as indicated in Fig. 2. The \( \Delta Q \) is expressed as (22).
\[
|\Delta Q| = \frac{V_o}{R} \int d_i T
\]
(22)
An expression for output ripple voltage is

\[
\Delta V_o = \frac{\Delta Q}{C_3} = \frac{I_o}{C_3} \frac{d_i}{d_i} T = \frac{V_o}{RC_3} \frac{d_i}{d_i} T
\]

III. STATE SPACE AVERAGED MODELING OF NOESLLC BASED ON S-T

A. Modeling of NOESLLC based on S-T

The state space equations for Fig. 1 (b) can be expressed as (24) and for Fig. 1 (d) can be written as (25).

Switch closed (24)

\[
\begin{align*}
\dot{i}_L &= \frac{V_{in}}{L} \\
\dot{V}_o &= -\frac{V_o}{C_3R}
\end{align*}
\]

Switch open (25)

\[
\begin{align*}
\dot{i}_L &= \frac{V_{in} - V_o}{L} \\
\dot{V}_o &= \frac{i_L}{C_3} - \frac{V_o}{C_3R}
\end{align*}
\]

Using the charge balance rule on \( C_1 \), Eq. (26) for \( T \) can be written. Here \( k \) denotes the status of the switch (\( d=1 \) when the switch is closed and \( d=0 \) when it is open).

\[
dC_2 dt + (1-d) |i_L| = 0
\]

As there are two capacitors in NOESLLC, with \( V_{C2} = V_{in} \), \( V_o \) alone can be chosen as a state space variable (not \( V_{in} \)). Similarly, with the inductor current \( i_{L1} \), entire space variables of the NOESLLC based on S-T can be chosen as \( i_L, V_c, x_1, \) and \( x_2 \). From (24), (25), and (26), the modeling of NOESLLC based on S-T in CCM may be written and is given by (27).

By (24), (25), and (26), the modeling of the NOESLLC based on S-T in CCM may be written by (27)

\[
\begin{bmatrix}
\dot{i}_L \\
\dot{V}_o
\end{bmatrix} =
\begin{bmatrix}
0 & -\frac{1 - d}{L} \\
\frac{1 - d}{C_3} & -\frac{1}{RC_3}
\end{bmatrix}
\begin{bmatrix}
i_L \\
V_o
\end{bmatrix} +
\begin{bmatrix}
\frac{1}{L} & 0
\end{bmatrix}
V_{in}
\]

B. Design of classical PI controller

A classical PI controller (shown in Fig. 3) is chosen for providing good output voltage regulation and reduced steady state errors for NOESLLC based on S-T. The dc output voltage is measured and compared with suitable reference output voltage that produces the voltage error
This error signal is applied to the PI controller to produce the control signal. This control signal is compared with carrier triangular signal to generate the Pulse Width Modulation (PWM) pulses for switches in NOESLLC based on S-T to keep the output voltage stable and minimize the steady state errors. The classical PI controller parameters, proportional gain ($K_p$) and integral times ($T_i$), are obtained with the help of Zeigler-Nichols tuning method. From this method, the NOESLLC based on S-T provides a sustained oscillation with ultimate gain ($K_{cr} = 0.00025$) and ultimate period ($P_{cr} = 0.0012$ s) resulting in the parameter values as $K_p = K_{cr}/2=0.00012$ and $T_i = P_{cr}/1.2=0.001$ s [27].

**IV. SIMULATION RESULTS**

**Table 1.** The table lists specifications of NOESLLC based on S-T.

<table>
<thead>
<tr>
<th>Parameters name</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>input voltage</td>
<td>$V_{in}$</td>
<td>12V</td>
</tr>
<tr>
<td>output voltage</td>
<td>$V_o$</td>
<td>-333.33V</td>
</tr>
<tr>
<td>Inductor</td>
<td>$L$</td>
<td>50µF</td>
</tr>
<tr>
<td>Capacitors</td>
<td>C1,C3,C2</td>
<td>25µH,60 µH, 200µH</td>
</tr>
<tr>
<td>nominal switching frequency</td>
<td>$f_s$</td>
<td>100KHz</td>
</tr>
<tr>
<td>load resistance</td>
<td>$R$</td>
<td>50Ω</td>
</tr>
<tr>
<td>average output current</td>
<td>$I_o$</td>
<td>-6.8A</td>
</tr>
<tr>
<td>duty ratio</td>
<td>$D$</td>
<td>0.482</td>
</tr>
<tr>
<td>peak to peak capacitor ripple</td>
<td>$\Delta V_o$</td>
<td>-0.1V</td>
</tr>
</tbody>
</table>
found that the diodes are open with ZVS (marked as circles in Fig. 4).

Figure 5 shows the simulated current waveforms of the NOESLLC based on S-T which clearly shows that the simulated values of the same converter are matching the theoretical values (refer Table 1). Figure 6 shows the simulated output and input current of the NOESLLC based on S-T which clearly shows that the simulated values of the same converter are matching the theoretical values (refer Table 1). Figure 7 shows the simulated output voltage and the input voltage responses of the designed converter using a classical PI controller for step change input voltage varied in the range from 12V to 15V and from 15V to 12V at time = 0.14 s. It is found that the output voltage of the NOESLLC based on S-T produced negligible overshoot and faster settling time.

Figure 6 shows the simulated current waveforms of the NOESLLC based on S-T. These waveforms give the gate voltage of switches $V_G$, current through the switch $I_{D1}$ and current through the diodes. It is found that the switches are closed with ZCS (marked as circles in Fig. 5) and the results match closely with the theoretical results (see Table 1). Figure 7 shows the output and input current of the NOESLLC based on S-T which clearly shows that the simulated values of the same converter are matching the theoretical values (refer Table 1). Figure 8 shows the simulated output voltage and the input voltage responses of the designed converter using a classical PI controller for step change input voltage varied in the range from 12V to 15V and from 15V to 12V at time = 0.14 s. It is found that the output voltage of the NOESLLC based on S-T produced negligible overshoot and faster settling time.
CONVENTIONAL NOESLLC:

Figure 9 shows MATLAB/Simulink model of the conventional NOESLLC. The output voltage and current through the switch of the conventional NOESLLC are shown in Fig. 10 and Fig. 11. The output voltage of the conventional NOESLLC converter produced $V_o = -36V$ for $V_{in} = 12V$, $R = 50 ohm$, $f_s = 100kHz$ and $d = 0.482$. The current through the switch gets more distorted (shown in Fig. 11) because of hard switching. Hence, the efficiency of this converter gets affected due to increased switching losses which cause EMI. Figure 12 shows the simulated output voltage and input voltage responses of the NOESLLC using a PI controller when the input voltage is varied from 12V to 15V and 15V to 12V. It is found that the output voltage of the NOESLLC using controller produced maximum overshoots of -26V and a settling time of 0.015 s.

Fig. 9. The MATLAB/Simulink model of a traditional NOESLLC.

Fig. 10. The simulated output voltage response of the traditional NOESLLC.

Fig. 11. Current through the switch of a traditional NOESLLC.

Fig. 12. Simulated output voltage response of the traditional NOESLLC using a PI controller is shown.

Time domain analysis and different input voltage variations of the NOESLLC based on S-T with and without controller are cataloged in Tables 2, 3 and 4. From these tables, it is clear that the designed converter performs well in the different working states.

Table 2. The summarizes the performance of the NOESLLC based on S-T for various input voltage.

<table>
<thead>
<tr>
<th>$V_{in}$ (V)</th>
<th>$V_o$ (V)</th>
<th>$I_o$ (A)</th>
<th>$P_o$ (W)</th>
<th>Output Ripple voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>-333.3</td>
<td>-6.6</td>
<td>2199.78</td>
<td>0.0036</td>
</tr>
<tr>
<td>14</td>
<td>-388.8</td>
<td>-7.776</td>
<td>3023.3</td>
<td>-0.01227</td>
</tr>
<tr>
<td>16</td>
<td>-444.4</td>
<td>-8.88</td>
<td>3946.272</td>
<td>-0.0139</td>
</tr>
<tr>
<td>18</td>
<td>-500</td>
<td>-10</td>
<td>5000</td>
<td>-0.0182</td>
</tr>
<tr>
<td>20</td>
<td>-555.5</td>
<td>-11.11</td>
<td>6160.5</td>
<td>-0.019</td>
</tr>
</tbody>
</table>
V. CONCLUSIONS

The design, analysis, operation and output voltage regulation of the new NOESLLC based on S-T with the classical PI controller has been shown through the MATLAB/Simulink software platform. Soft switching analysis of the NOESLLC based on S-T was performed, which can lead to fewer switching losses. The NOESLLC based on S-T was found to produce good efficiency, a high output voltage with minimum duty ratio, and fewer ripples in the capacitor voltage and inductor current in comparison with the traditional NOESLLC. The results reported here prove the proficiency of NOESLLC based on S-T with different input/output voltage and duty cycle operating conditions in comparison with the traditional NOESLLC. In addition, the NOESLLC based on S-T with the classical PI controller was found to produce good dynamic performance in line and load variations, superior output voltage regulation and fine time domain specification analysis over the traditional NOESLLC. Therefore, it was found to be more suitable for high voltage applications. Further, a non-linear controller is also being developed for the NOESLLC based on S-T to improve its performance and experimental model is under construction.

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