MODELLING AND CONTROL OF THREE PHASE ASYMMETRIC CASCADED H-BRIDGE MULTILEVEL INVERTER USING ADVANCED PULSE WIDTH MODULATION TECHNIQUE

D. Periyaazhagar
Bharath University, Chennai 600 073, Tamil Nadu, India
+91-9843664423 periyaazhagar@gmail.com

G. Irusapparajan
Mailam Engineering College, Mailam 604 304, Tamil Nadu, India
+91-9791780404 irusgkm@gmail.com

N. Prabaharan
VIT University, Vellore 632014, Tamil Nadu, India
+91-9750785975 prabaharan.nataraj@gmail.com

Abstract: Multilevel inverter is one of the power electronic devices used in high power applications, which are effective for medium voltage and high power applications, with the additional benefit of reducing total harmonic distortion and lower switching stress, hence decreasing the size of the filter and avoiding the use of bulk input transformer. It generates the staircase AC output voltage from the input DC sources. Multilevel inverters can be classified into two types such as Asymmetrical multilevel inverter and Symmetrical multilevel inverter. The proposed multilevel inverter is an asymmetrical type. Advanced pulse width modulation scheme is utilized in this paper, a new asymmetrical three-phase multilevel inverter is proposed using trinary DC source cascaded H Bridge. This trinary DC source cascaded H Bridge can produce nine level output voltage and it is tested with both R and RL load. Simulation of a proposed three phase multilevel inverter is verified using MATLAB-SIMULINK. The strength of the proposed multilevel inverter is verified by the experimental test board results using an FPGA. This approach is predictable to be valuable for higher power and higher voltage applications.

Key words: Multilevel inverter, pulse width modulation, total harmonic distortion, cascaded h-bridge multilevel inverter, trinary DC source.

1. Introduction.

The necessity for high power converter in industry has improved in modern years. Multilevel inverters have established as easy replacements of low power converter in many industries. Multilevel inverter contains a group of power semiconductor devices and a set of source, voltage apparatuses like capacitors or independent sources. The basic conception of these inverters depends on the connection of series/parallel of power semiconductor devices and input DC sources to create a stepped or staircase output voltage waveform. The multilevel inverter plays a substantial role in enhancing the excellence of high power and medium voltage distribution networks, high power conditioning systems, adjustable speed drive systems etc [1].

In [2,3], Incorporation scheme was recommended for removing the harmonics of asymmetrical cascade H-bridge multilevel inverter has discussed. The recommended incorporated scheme was united with two intelligence approaches that were fuzzy logic and PSO algorithm. The harmonic removal concert of the recommended scheme was investigated with seventh level asymmetrical cascade multilevel inverter (ACMLI). An industrial controller has considered for two and three level inverter which has altered to work on an asymmetrical nine level active power filter. The controller has now exceptional to make all compulsory tasks for the accurate operation of the active power filter, such as current harmonic removal and elimination of higher frequency noise. The lower switching frequency action of nine level inverters was an essential benefit in the presentation of the industrial controller. A matrix converter is an AC to AC power converting topologies that has established extensive research attention as another to traditional AC to DC to AC converter. A matrix converter is capable to convert energy from an AC source (Alternating) to an AC load without the requirement of a huge and limited lifetime energy storage system [4]. Shunt interleaved electrical drive structures containing of numerous parallel medium voltage back-to-back converters allow power grades of tens of MVA, lesser current distortions, and an exact smooth air gap torque. To chance inflexible reliability and accessibility goals despite the bulky parts count, the modularity of the drive structure essentials to be exploited and a meet fault handling scheme that permits the exclusion and isolation of faulted threads is compulsory [5, 6]. The control of four quadrant converters of electric traction vehicles served by an AC railway grid has to chance exact restrictive limitations with concern to harmonics content and strength. The experiment is increased by constantly changing the location dependent grid impedance and voltage harmonics contents previously limited in the grid voltage. Fault tolerance capability of the hexagram
Inverter motor drive systems, due to its single interconnecting nature, the hexagram inverter can tolerate single leg failure deprived of adjusting the power circuit topologies [7, 8]. The trinary DC Source multicarrier based PWM technology is used to produce a nine level ac output voltage with various PWM scheme. In [9], Phase shift pulse width modulation system is preferred as the finest modulation scheme for a 20MW voltage source converter HVDC with concern of the total harmonic distortion of the system output voltage. In [10], the investigation of the switching status of each unit section of a cascaded multilevel inverter exposes that the operating condition of the switching of a chopper arm causes avoidable switching beneath the existing USPWM. Single phase 5level inverter organized by two different PWM switching systems and this projected PWM switching are planned based on smallest switching power loss and smallest harmonic distortion [11].

2. Proposed Trinary DC source multilevel inverter.

The proposed three-phase trinary DC source cascaded asymmetrical multilevel inverter consists of three single phase multilevel inverter. The each single phase unit contains two full bridges with unequal DC source. The first full bridge holds the input DC source of 1Vdc and the second full bridge holds the input DC source 3Vdc as presented in Fig. 1. Each input DC source is connected in series to make a proposed three phase MLI. Each inverter generates a three dissimilar (unequal) output voltage levels, such as positive (+Ve), zero (0) and negative (-Ve) levels by different groupings of the four power semiconductor switches S1, S2, S3 and S4. Whenever switches, S1 and S4 are turned ON, then the inverter output voltage is positive level (+Ve); whenever the switches S2 and S3 is turned ON, then the inverter output voltage is negative level (-Ve); whenever either pair of switches (S1 and S2) or (S3 and S4) is turned ON, then the output voltage will be at zero level (0).

Then the output voltage of first bridge can be made equal to the −1Vdc, 0, or 1Vdc, correspondingly the output voltage of second bridge can be made equal to the −3Vdc, 0, or 3Vdc by turning ON and turning OFF its power semiconductor switches properly. Consequently, the output voltage of the inverter values for −4Vdc, −3Vdc, −2Vdc, −1Vdc, 0, 1Vdc, 2Vdc, 3Vdc, 4Vdc, 1Vdc, can be generated. Table 1 represents the switching sequence of proposed multilevel inverter.

The lower inverter (HB2) produces a necessary output voltage with three levels, and then the upper inverter (HB1) adding or subtracting one level from the fundamental output voltage wave to produce stepped waves. Following represents the switching sequence of three phase nine level inverter with R Phase and other two-phase (Y and B Phase) are similar to R Phase. To produce a stair case/ stepped output voltage, the following steps should be followed.

**Step 1:** For an output voltage level, \( V_{out}=0 \)Vdc, the power semiconductor switches S2 and S4 are tuned on at both full bridge inverter.

**Step 2:** For an output voltage level, \( V_{out}=1 \)Vdc, the power semiconductor switches S1 and S4 are turned on on at upper full bridge, S2 and S4 are turned on at lower full bridge inverter.

**Step 3:** For an output voltage level, \( V_{out}=2 \)Vdc, the power semiconductors switches S2 and S3 are turned on at upper full bridge, S1 and S4 are turned on at lower full bridge inverter.

**Step 4:** For an output voltage level \( V_{out}=3 \)Vdc, the power semiconductor switches S2 and S4 are turned on at upper full bridge, S1 and S4 are turned on at lower full bridge inverter.

**Step 5:** For an output voltage level \( V_{out}=4 \)Vdc, the power semiconductor switches S1 and S4 are turned on

The output voltage of the first bridge is indicated by Vdc and the second full bridge is indicated by 3Vdc. In the proposed inverter circuit topologies, if \( m \) number of cascaded H bridge segment has unequal DC sources in order of the power of 3, a predictable output voltage levels are given as

\[
V_m = 3^m, m = 1, 2, 3, \ldots
\]
at upper full bridge, S1 and S4 are turned on at lower full bridge inverter.

**Step 6:** For an output voltage level $V_{out} = -1\,V_{dc}$, the power semiconductor switches S2 and S3 are turned on at upper full bridge, S2 and S4 are turned on at lower full bridge inverter.

**Step 7:** For an output voltage level $V_{out} = -2\,V_{dc}$, the power semiconductor switches S1 and S4 are turned on at upper full bridge, S2 and S3 are turned on at lower full bridge inverter.

**Step 8:** For an output voltage level $V_{out} = -3\,V_{dc}$, the power semiconductor switches S2 and S4 are turned on at upper full bridge, S2 and S3 are turned on at lower full bridge inverter.

**Step 9:** For an output voltage level $V_{out} = -4\,V_{dc}$, the power semiconductor switches S2 and S3 are turned on at upper full bridge, S2 and S3 are turned on at lower full bridge inverter.

4. **Advanced pulse width modulation technique.**

The sinusoidal PWM technique is most widely used PWM technique but it has the drawback of producing the low fundamental RMS output voltage. Due to overcome the drawback, advanced pulse width modulation has been developed. In this work, advanced PWM with multicarrier arrangement is used for generating the triggering pulse for proposed trinary sequence based CHBMLI. For an ‘m’ level inverters in bipolar multi-carrier techniques, ‘m-1’ carriers with same frequency $f_c$ and same peak to peak amplitude $A_c$ are required [12, 13]. The reference waveform has amplitude of $A_m$ and frequency of $f_m$, and it is placed at the both cycles. The reference wave is continuously compared with each triangular carrier signals. Whenever the reference wave is greater than carrier signals leads to activate a device corresponding to those carriers otherwise the semiconductor device is switched off. There are many advanced pulse width modulation control techniques has discussed in literature. In this paper, Trapezoidal PWM is discussed which is one of the techniques of it.

The triggering signals are generated by comparing a triangular wave carrier signals with a modulating trapezoidal reference wave. This type of modulation techniques increases the peak fundamental RMS output voltage. The trapezoidal reference wave signal can be achieved from a triangular wave carrier signal by restrictive its magnitude to $A_c$ which is interrelated to the peak value of $A_{r(max)}$ is given by

$$A_r = \alpha A_{r(max)} \quad (3)$$

Where

$\alpha$ is called as the triangular wave factor.

Because the waveform becomes a triangular wave signal when $\alpha=1$. Then the modulation indices $M_a$ is given by

$$M_a = \frac{A_r}{A_c} = \frac{\alpha A_{r(max)}}{A_c} \quad (4)$$

The angle of the flat portion the trapezoidal reference wave is given by

$$2\phi = (1-\alpha)\pi \quad (5)$$

For stable values of $A_{r(max)}$ and $A_c$, the magnitude and level of output voltage changes with respect to the modulation index. Here, $A_{r(max)}$ is called as peak amplitude of trapezoidal reference wave. $A_c$ is called as peak amplitude of carrier triangular signals. Here, trapezoidal wave signal is used as a reference signal and triangular wave is used as carrier signal. There are many control techniques are possible, some of those techniques are discussed in this paper which is given below:

4.1 Phase disposition pulse width modulation technique (PD).

4.2 Phase opposition disposition pulse width modulation system (POD).

4.3 Alternate phase opposition disposition pulse width modulation system (APOD).

4.4 Carrier overlapping pulse width modulation system (COP).

4.5 Variable frequency pulse width modulation system (VF).

The formula of Amplitude modulation indices ($M_a$) for phase disposition PWM, Phase Opposition Disposition PWM, Alternate Phase Opposition Disposition PWM and Variable Frequency PWM is given below

$$M_a = \frac{4A_m}{(m-1)A_c} \quad (6)$$

For the carrier overlapping PWM

$$M_a = \frac{A_m}{(2.5)^{m-1}A_c} \quad (7)$$

Here, $A_m$-Amplitude of a Modulating signal (Reference Signal), $A_c$-Amplitude of a carrier signal, $m$ - output level, $M_a$-Modulation index.

4.1 In Phase Disposition Pulse Width Modulation Technique

For an m-level inverter, (m-1) carriers with the same carrier frequency of $f_c$ and the same amplitude of carrier signal is $A_c$ are required. In phase disposition pulse width modulation technique (PD), all carriers are in phase with each other and it has same amplitude. The carrier wave arrangement of three-phase multilevel inverter with trapezoidal reference is shown in Fig. 2(a).
4.2 Phase Opposition Disposition Pulse Width Modulation Technique

For an m-level inverter, (m-1) carriers with the same carrier frequency of \( f_c \) and the same amplitude of carrier signal is \( A_c \) are required. Phase opposition disposition pulse width modulation technique (POD), all carriers are in phase with above and below the modulating signals in zero values. These carriers which below the zero values are 180 degrees out of phase width. The carriers’ wave arrangement of three-phase multilevel inverter with trapezoidal reference is shown in Fig. 2 (b).

4.3 Alternate Phase Opposition Disposition Pulse Width Modulation Technique

For an m-level inverter, (m-1) carriers with the same carrier frequency of \( f_c \) and the same amplitude of carrier signal is \( A_c \) are required. Alternate phase opposition disposition pulse width modulation technique (APOD), the carriers are 180 degree phase displaced with its neighbor carrier. The carrier wave arrangement of a three phase multilevel inverter with trapezoidal references is shown in Fig. 2 (c).

4.4 Carrier Overlapping Pulse Width Modulation Technique

All carriers have the same frequency \( f_c \) and same amplitude \( A_c \) is disposed such that their bands occupy overlapping with each other carriers. The overlapping vertical distances between each carrier are \( A_c/2 \) which is shown in Fig. 2 (e). Amplitude of the reference waveform is \( A_0 \) and frequency is \( f_0 \) and it is centered in the middle of the carrier signals.

4.5 Variable Frequency Pulse Width Modulation Technique

The number of switching pulse for upper and lower devices of chosen multilevel inverter is much more than that of intermediate switches in phase disposition pulse width modulation using a constant frequency carrier. In order to equalize the number of switching for all the switches, variable frequency pulse width modulation technique are used as shown in Fig. 2 (d) in which all the carrier frequencies of the intermediate switches is properly increased to balance the number of switching for all the switches.
5. Simulation results and discussion.

A trinary DC source cascaded asymmetrical three-phase multilevel inverter for generating the nine level output voltage is modeled in MATLAB-SIMULINK using power systems block set. The proposed multilevel inverter simulation circuit is shown in Fig. 3. Simulations result of %THD is carried out for different values of m, ranges from 0.8 to 1 using the FFT plot. Table 1 shows the values of %THD for R and RL load in different carrier arrangement. Table 2 shows the fundamental RMS output voltage of Vrms of proposed MLI in both R and RL load for various carrier arrangements during the modulation indices range of 0.8 to 1.

5.1 R Load

Fig. 4 represents the output voltage created by carrier based PWM control with trapezoidal reference for R Load. For a modulation indices (m = 0.85), it is observed from the Fig. 5(a), 5(b), 5(c), 5(d) and 5(e)) the harmonic energy level is governing in: Fig. 5(a) characterizes the harmonic energy level in PD PWM techniques shows 5th, 20th, and 40th order of harmonic. Fig. 5(b) characterizes the harmonic energy level in POD PWM techniques shows 5th, 19th, 20th, 29th, 31st and 40th order of harmonic. Fig. 5(c) represents the harmonic energy level in APOD PWM techniques shows 5th, 7th, 29th, 31st, 35th, 37th and 39th order of harmonic. Fig. 5(d) characterizes the harmonic energy level in COP PWM techniques shows 5th and 40th order of harmonic. Fig. 5(e) characterizes the harmonic energy level in VFPWM techniques shows 5th and 39th order of harmonics.

5.2 RL Load

Fig. 6 represents the output voltage created by carrier based PWM control with trapezoidal reference for RL Load. For a modulation indices (m = 0.85), it is observed from the Fig. 7(a), 7(b), 7(c), 7(d) and 7(e)) the harmonic energy level is governing in: Fig. 7(a) characterizes the harmonic energy level in PD PWM techniques shows 5th and 39th order of harmonic. Fig. 7(b) characterizes the harmonic energy level in POD PWM techniques shows 5th, 20th and 40th order of harmonic. Fig. 7(c) represents the harmonic energy level in APOD PWM techniques shows 5th, 7th, 29th, 31st, 35th, 37th and 39th order of harmonic.
37th and 39th order of harmonic. Fig. 7(c) characterizes the harmonic energy level in COP PWM techniques shows 5th and 40th order of harmonic. Fig. 7(d) characterizes the harmonic energy level in VF PWM techniques shows 5th, 11th, 19th, 27th, 29th, 39th and 40th order of harmonics. Table 1 and Figure 8 represent the THD contrast of IPD, POD, APOD, COP and VF pulse width modulation techniques with R and RL load no more than one pulse modulation techniques such as POD in R load (Phase Opposition Disposition) it hold minimum quantity of harmonic distortion. Table 2 and Figure 9 represent the V\textsubscript{RMS} contrast of IPD, POD, APOD, COP and VF pulse width modulation techniques with R and RL load no more than one pulse modulation techniques such as COP in R load (Carrier Overlapping) it hold maximum quantity of fundamental RMS output voltage.

Fig. 4. Output voltages created by All Carrier based PWM control with Trapezoidal reference for R load

![Fig. 4](image)

Fig. 5. FFT plot for output voltage of PWM control with Trapezoidal reference with R Load: (a) PD PWM system; (b) POD PWM system; (c) APOD PWM system; (d) COP PWM System; (e) VF PWM System
Fig. 6. Output voltages created by All Carrier based PWM control with Trapezoidal reference for RL Load

(a) Fundamental (50Hz) = 89.01, THD= 17.69%
(b) Fundamental (50Hz) = 89.01, THD= 17.69%
(c) Fundamental (50Hz) = 99.41, THD= 23.74%
(d) Fundamental (50Hz) = 89.5, THD= 17.58%
(e) Fundamental (50Hz) = 89.45, THD= 17.76%

Fig. 7. FFT plot for output voltage of PWM control with Trapezoidal reference with RL Load: (i) IPD PWM system; (ii) POD PWM system; (iii) COP PWM System; (iv) APOD PWM system; (v) VF PWM System

Fig. 8. % THD Vs Modulation Indices
6. Experimental results.

The prototype model of a new asymmetrical three phase cascaded H Bridge multilevel inverter with trinary DC source for both R and RL loads are implemented using FPGA. The FPGA is a best choice of hardware test board development due to its capability to produce exact results at a greater computational speed. A new asymmetrical three phase multilevel inverter experiment has been implemented with the proposed carrier based PWM techniques. Triggering signal is produced by matching trapezoidal pulse width modulation with triangular carriers’ wave. The prototype model of asymmetric multilevel inverter is implemented with R Phase only. It is developed using IGBTs as the semiconductor switching devices and it’s shown in Fig. 10. The PWM pulses are produced using Multicarrier PWM like Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternate Phase Opposition Disposition (APOD) techniques using Xilinx arrangement originator, which is visualized in Fig. 11. The nine level output voltage waveform with the FFT plot for the proposed trinary CHBMLI in the modulation index of 0.95 with PD and POD technique are shown in Fig. 12 and 13 respectively. The experimental outcomes prove that the proposed multilevel inverter structure has more hands-on feasibility for practical implementation.
7. Conclusion.
A trinary based asymmetric three phase cascaded H Bridge multilevel inverter with R and RL load has been discussed in this article. It is observed that phase opposition disposition PWM scheme (RL Load) with trapezoidal reference delivers better output waveform with relatively low total harmonic distortion and carrier overlapping PWM scheme (R Load) with trapezoidal reference delivers relatively greater fundamental RMS output voltage ($V_{RMS}$). The performance parameter like, Total Harmonic Distortion (THD) and Fundamental RMS output voltage ($V_{RMS}$) are calculated and tabulated. The simulation circuit and prototype model are accomplished to show the strong point of the proposed new asymmetrical three phase multilevel inverter with trinary DC source cascaded H Bridge. This topology
could be tested with renewable energy sources like photovoltaic panel or wind energy in future. Also, it could be tested with other pulse width modulation technique like space vector pulse width modulation or soft computing algorithms.

References


